Doctoral Dissertation

Ultra-Low Power Ternary CMOS Platform for Physical Synthesis of Multi-Valued Logic and Memory Applications

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2017

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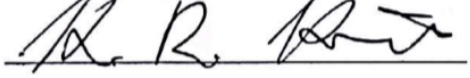
A dissertation
submitted to the Graduate School of UNIST
in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Sunhae Shin

07. 01. 2017 of submission

Approved by



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Abstract

Motivation of this work is to provide feasible, scalable, and designable multi-valued logic (MVL) device platform for physical synthesis of MVL circuits. Especially, ternary device and its general logic functions are focused, owing to most efficiently reduced circuit complexity per radix (R) increase. By designing the OFF-state constant current, not only the standby power (P_S) issue of additional intermediate state is overcome, but also continuous supply voltage (V_{DD}) scaling and dynamic power (P_D) scaling are possible owing to single-step *I-V* characteristics.

By applying a novel ternary device concept to CMOS technology with OFF-state current mechanism of band-to-band tunneling (BTBT) currents (I_{BTBT}) and subthreshold diffusion current (I_{sub}), the logic changes from binary to ternary are confirmed using mixed-mode device simulation. I experimentally demonstrate ternary CMOS (T-CMOS) and verified its low-power standard ternary inverter (STI) operation by designing channel profiles in conventional binary CMOS. The realized complementary ternary *n/p*MOS (T-*n/p*MOS) have fully gate bias (V_G)-independent and symmetrical I_{BTBT} of ~10 pA/μm based on proven ion-implantation process, which produces stable and designable intermediate state (V_{OM}) at exactly $V_{DD}/2$.

To present T-CMOS design frameworks in terms of static noise margin (SNM) enhancement and ultra-low power operation, I develop the compact model of T-CMOS and verify the physical model parameters with experimental data. Through the feasible design of I_{sub} with abrupt channel profile based on low thermal budget process, STI has a SNM of 283 mV (80 % of ideal SNM) at V_{DD}= 1V operation and intermediate state stability of $\Delta V_{OM} < \pm 0.1$V, even considering the random-dopant fluctuation (RDF) of 32 nm and 22 nm technology. Continuous V_{DD} scaling below 0.5V (SNM= 40% at V_{DD} = 0.3V) enables STI operation with ultra-low P_D and P_S based on exponentially reduced I_{BTBT} currents.

As MVL and memory (MVM) applications, minimum(MIN)/maximum(MAX) gates, analog-to-digital converter (ADC) circuit, and 5-state latch are studied with T-CMOS compact model. Especially ADC circuits revolutionary decreases number of device and circuit interconnection with 9.6% area of binary system.

Keywords—Multi-valued logic (MVL), standby power, dynamic power, band-to-band tunneling (BTBT), subthreshold diffusion, ternary CMOS (T-CMOS), standard ternary inverter (STI), intermediate state, Static noise margin (SNM), random-dopant fluctuation. (RDF), minimum(MIN) gate, maximum(MAX) gate, analog-to-digital converter (ADC), multi-valued memory (MVM).

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Nomenclature and Predicate

ADC	Analog-to-digital converter
BTBT	Band-to-band tunneling
CMOS	Complementary metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
***n*MOS**	*n*-type MOSFET
***p*MOS**	*p*-type MOSFET
CNTFET	Carbon nanotube field-effect transistor
DECMOS	Depletion/enhancement mode CMOS
EOT	Equivalent oxide thickness
GIDL	Gate-induced drain leakage
HDD	Highly doped drain
IoT/IoE	Internet of things/everything
ITRS	International technology roadmap for semiconductors
LDD	Lightly doped drain
LSTP	Low standby power
MAX	Maximum gate
NMAX	Not maximum gate
MIN	Minimum gate
NMIN	Not minimum gate
MVL	Multi-valued logic
MVM	Multi-valued memory
NDR	Negative differential resistance

***n*NDR**	*n*-type NDR
***p*NDR**	*p*-type NDR
NM	Noise margin
OVL	OFF-leakage variation
PDP	Power-delay-product
PDR	Positive differential resistance
PECVD	Plasma-enhanced chemical vapor deposition
PVCR	Peak-to-valley current ratio
QDGFET	Quantum dot field-effect transistor
RITD	Resonant interband tunneling diode
RTA	Rapid thermal annealing
SCEs	Short channel effects
SNM	Static noise margin
SSW	Subthreshold swing
STI	Standard ternary inverter
PTI	Positive ternary inverter
NTI	Negative ternary inverter
TAT	Trap-assisted tunneling
T-CMOS	Ternary CMOS
T-*n*MOS	Ternary *n*MOS
T-*p*MOS	Ternary *p*MOS
T-FinFET	Ternary FinFET
TFET	Tunneling field-effect transistors
VTC	Voltage transfer curve

Chapter 1. Introduction

1.1 Challenges of CMOS Technology

Digital computing systems based on binary logic function have been progressed by achieving higher bit density and better performance through the continuous scaling of complementary metal-oxide-semiconductor (CMOS) devices. During the miniaturization of sub-30 nm CMOS technology regime, however, the increase of bit density has been constrained by the power density limits, especially stand-by power (P_S) consumption owing to OFF-leakage current in planar structure [1]. While this P_S scaling issue has been mitigated by employing nonplanar tri-gate fin structures from 22-nm and 14-nm technology node [2],[3], operation voltage (V_{DD}) scaling for dynamic power consumption ($P_D \sim V_{DD}^2$) has been saturated around 1 V owing to the non-scaling factor of threshold voltage ($V_T = 0.3 \times V_{DD}$) in CMOS device. It should be noted that the integration density is not determined by a minimum device size ($L_{min} \sim$ 1.5 nm) but by a power density limit (< 100 W/cm^2) from a theoretical study [4] and the international technology roadmap for semiconductors (ITRS) [5].

As the alternatives for ultimate low power circuit and device, the subthreshold logic and tunneling field-effect transistors (TFETs) have been intensively studied. However, the subthreshold logic has been struggling with the static-energy limitation on planar CMOS owing to short channel effects (SCEs) [6], and the logic switching and noise margin (NM) degradation by the process variation on multi-gate FETs [7]. In the TFETs, many technical challenges such as low interface trap density on gate stacks, abrupt source doping profiles, and suppression of OFF-state ambipolar current should be solved [8]. With a fundamental viewpoint of information density, binary logic device have to increase circuit and system complexity for Big Data information processing, internet of things/everything (IoT/IoE), and neuromorphic chip by consuming huge energy, thereby cannot overcome power scaling limit

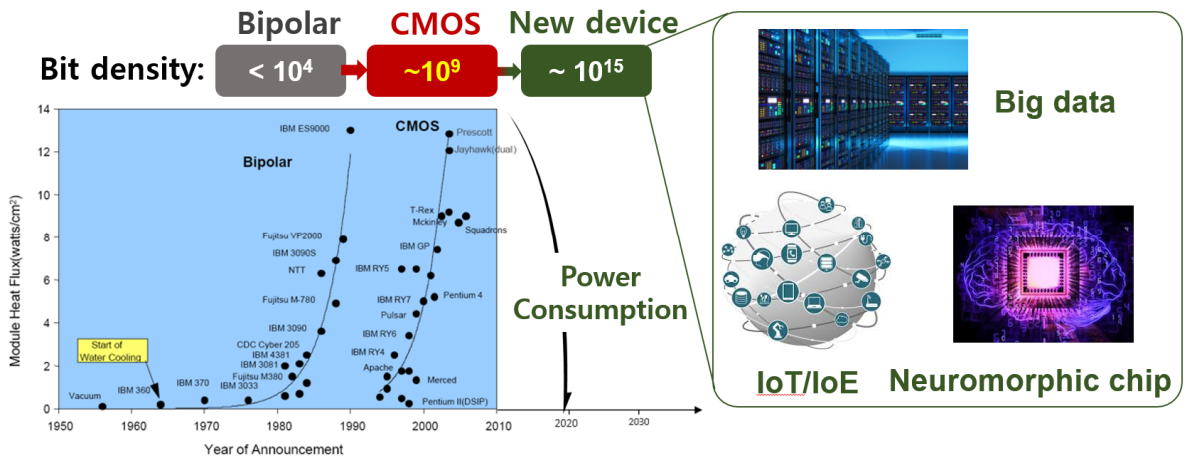


Figure 1.1. Necessity of new semiconductor device technology

fundamentally. The replacement of bipolar technology used in semiconductors in the 1970s with CMOS technology in the 1980s was also a matter of power consumption, therefore, new device technology is required to solve the current energy consumption problem as shown in Fig. 1.1.

1.2 Multi-Valued Logic

For the breakthrough of power-density limit of conventional binary system, multi-valued logic (MVL) has been considered as one of the promising architectures [9]. The MVL system can dramatically reduce energy for high-density data processing through the improvement of information density and reduction of system complex with same effect as road-lane expansion (Fig. 1.2). Theoretically, the MVL with *R*-logical bit (radix) has following advantages:

- To represent *n*-bit binary process, it only takes $n \times \log_R 2$ bit on *R*-logical process.
- The circuit complexity and number of interconnection are proportional to $\log_R 2$.
- The P_D is reduced by $1/(R\text{-}1)^2$ times from P_D= switching activity (α) × frequency (f) × load capacitance (C_L) × operation voltage $(V_{DD}/(R\text{-}1))^2$.
- The propagation delay is decreased by $1/(R\text{-}1)$ times compared with binary logic under same operating current/voltage.

The first introduction of MVL is "unknown" (or possible) state by Jan Lukasiesicz in 1920 [10], since then the mathematical approaches of MVL were extended into two concepts of finite (ternary, quaternary, etc.) [11] and infinite number of logic levels (e.g. fuzzy logic) [12]. However, in spite of the introduction of MVL concept, the key issue that MVL technology has not been realized over the past 100 years is the lack of feasible and designable device platform for circuit design. Thus, the early stage of finite MVL researches have focused on the software-oriented system computing fields with a basis of the mathematical theory due to the lack of hardware technology. Therefore, for the realization of MVL system, feasible, designable and low power device platform should be construct.

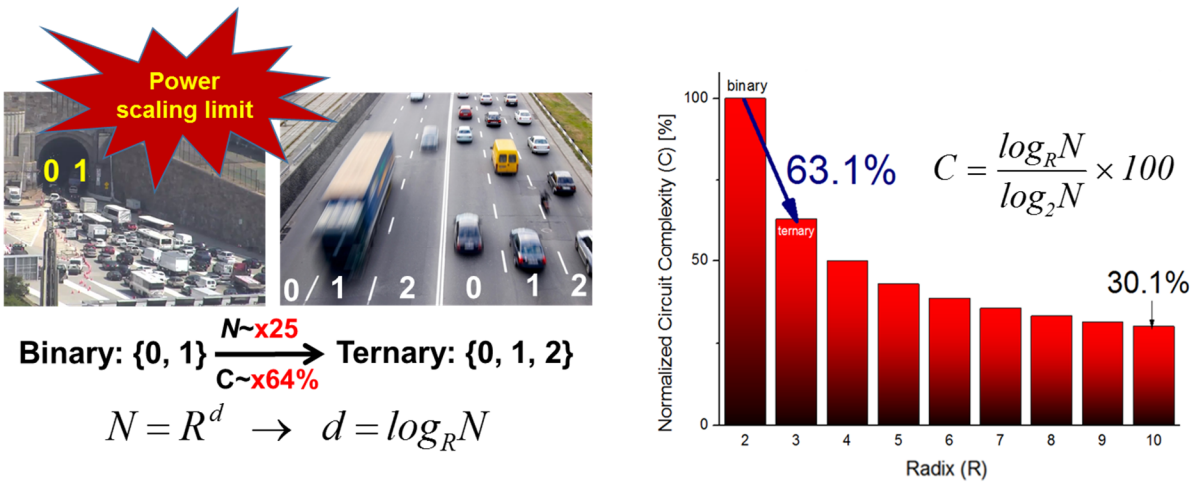


Figure 1.2. Reduced circuit complexity of MVL system

1.3 Previous Research Works of Ternary Devices/Circuits

Ternary system has been attracting much attention owing to most efficiently reduced circuit complexity per radix (R= 3) increase, which only takes $\log_3(2^n) = n \times 63.1\%$ bit to represent n-bit binary number. In particular, as a basic building block of the general three-valued logic function, intensive researches have been performed to realize standard ternary inverter (STI). Figure 1.3 shows the voltage transfer curve (VTC: V_{OUT}-V_{IN}) of STI with truth-table and symbol marked "T" to distinguish it from binary inverter.

In the 1990s, MVL circuits have been developed based on current-mode transistor operation, which has disadvantages of P_S dissipation and the output impedance variation [13]. To overcome these limitations, the voltage-mode MVL have been a mainstream research in recent years [14]. The following subsections introduce previous works from other research groups focusing on voltage mode STI.

1.3.1 Ternary Circuits Based on Binary Devices with Multi-V_{DD}

An intuitive approach to binary device-based ternary circuit design is to introduce additional voltage sources and access elements into existing binary circuits. In [15], additional voltage source 'C' and access element 'R' (R, I_{ON}/V_{DD} < R < I_{OFF}/V_{DD}) are utilized, however, it resulted in deteriorating both delay and power in the additional state (Fig. 1.4(a)). To address this issue, the research [16] proposed multi-V_T-based depletion/enhancement mode CMOS (DECMOS) circuits (Fig. 1.4(b)).

Figure 1.5(a)-(c) illustrates the I_{OUT}-V_{OUT} characteristics of DECMOS STI for low, intermediate, and high states transfer. At here, the intersections of I_{OUT}-V_{OUT} curves become logical states as with binary

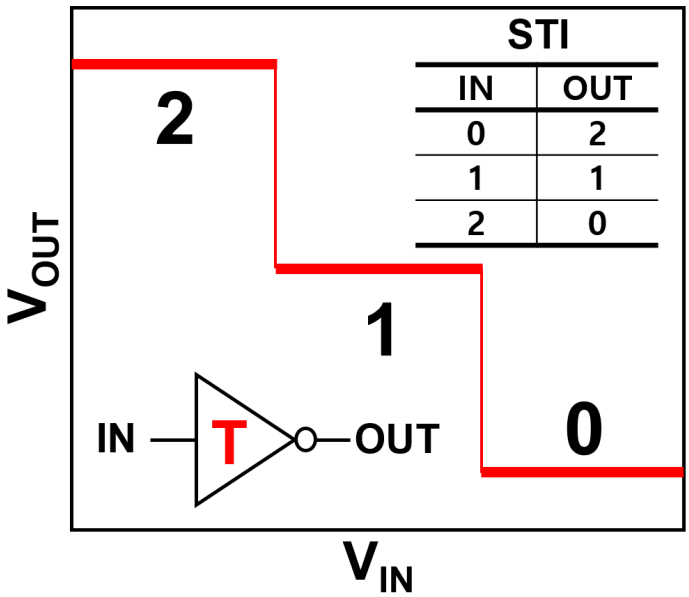
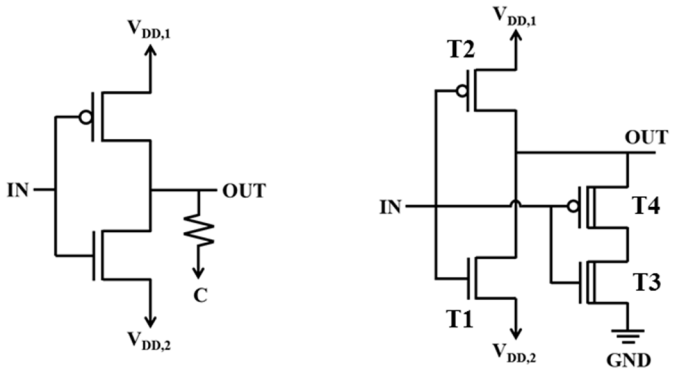


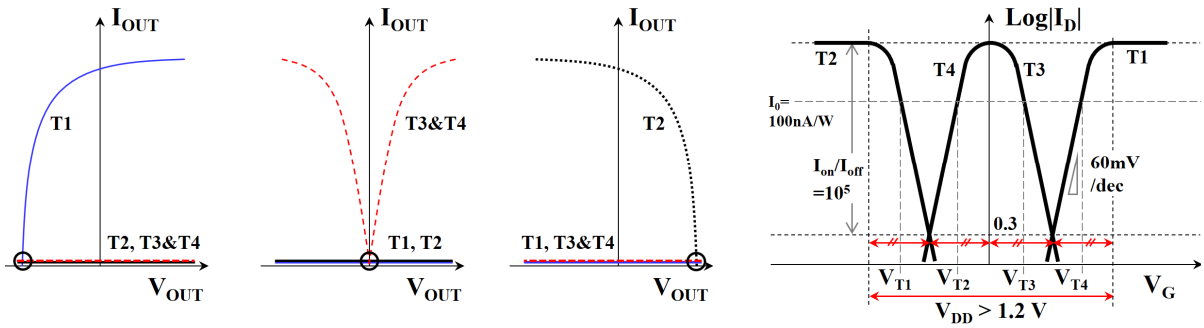
Figure 1.3. VTC, truth table, and symbol of STI

inverter. When the input voltage is high (V_{IN} = 1 V), transistor T1 is turned ON while T2 and T4 are turned OFF, which result in high output voltage (V_{OUT}= -1 V, logic 0). In the same manner, when the input voltage is high (V_{IN}= -1 V), T2 is turned ON while T1 and T3 is turned OFF, which results in low output voltage (V_{OUT}= 1 V, logic 2). If the input voltage is intermediate (V_{IN}= 0 V), both T2 and T4 are turned ON while both T1 and T3 are turned OFF; output voltage is also intermediate (V_{OUT}= 0 V, logic 1). Since the access transistor connected to the transfer voltage source operates in the ON state, it is comparable to the binary inverter in terms of speed, and the other transistors maintain the OFF-state, thereby suppressing the static current. However, to take this advantage, multi-V_T devices should be designed with $I_{ON}/I_{OFF} > 10^5$ to express ON/OFF state sufficiently. It requires high V_{DD} (= 2 V in [17]) compared to single-V_T-based binary CMOS circuit/system. When V_{DD} scaling is considered to solve P_D increase due to high V_{DD}, an increase in OFF current is inevitable and P_S increases. Figure 1.5(d) shows the V_{DD} scaling limit based on the transfer log(I_{OUT})-V_{IN} characteristics of the DECMOS STI. At here, $V_{DD} \geq 4\times SSW\times\log(I_{ON}/I_{OFF})$ = 1.2V (± 0.6V) can be expected by applying conditions of ideal CMOS subthreshold swing (SSW) = 60mV/dec and I_{ON}/I_{OFF}= 10^5. In addition, logic circuit design based on DECMOS requires five transistors in the positive / negative ternary inverter (PTI / NTI) circuit and eight transistors in the not minimum (NMIN) / not maximum (NMAX) circuit. The area of the unit gate and the circuit complexity increase.



(a) (b)

Figure 1.4. STI circuits based on binary CMOS with Multi-V_{DD}: (a) Ref. [15] and (b) Ref. [16].



(a) (b) (c) (d)

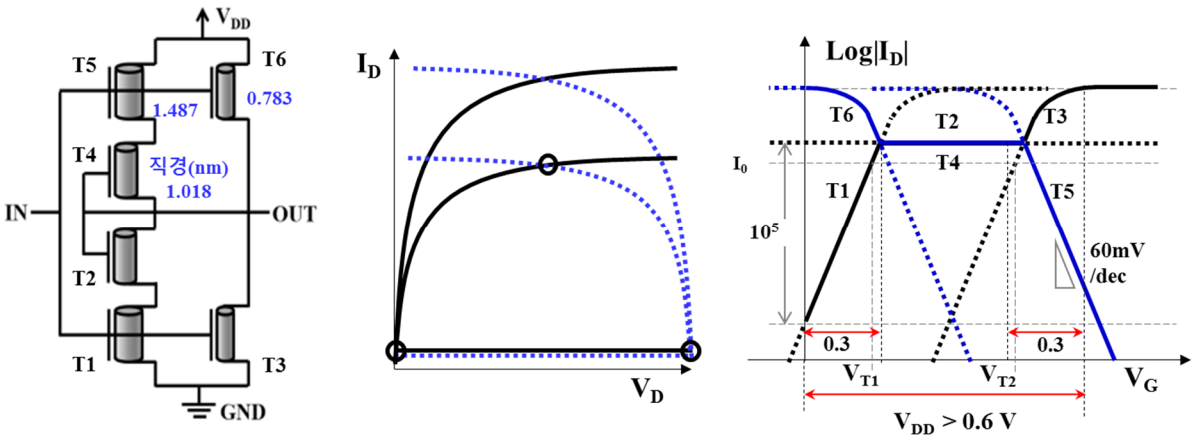
Figure 1.5. I_{OUT}-V_{OUT} characteristics for (a) low, (b) intermediate, and (c) high-state transfer and (d) transfer I_{OUT}-V_{IN} characteristics of DECMOS and its V_{DD} scaling limits.

1.3.2 Ternary Circuits Based on Binary Devices with Multi-V_T

Another approach to ternary logic circuit design using binary devices is to implement an intermediate state through voltage dividing with single-V_{DD}. The V_{IN}-independent constant current (I_{CON}) are required to obtain constant intermediate state in a specific input interval. The researches of forming an I_{CON} have been developed from serially connected resistor [17]-[19] to saturation-mode transistors [20]-[21].

Figure 1.6(a) shows STI circuit based on multi-V_T carbon nanotube (CNT) field-effect transistor (FET) with single V_{DD}. As an alternative to solve the area size problem of the multi-V_T CMOS-based ternary circuits, CNTFETs are widely used in MVL circuit/system design since they can dramatically reduce device size, and high V_T margin compared to the CMOS is also advantageous for the multi- V_T design. For the STI design, CNT diameter (D)= 1.487 nm for V_T= ± 0.289 V (T1/T5), D=1.018 nm for V_T= ± 0.428 V (T2/T4), and D= 0.783 nm for V_T= 0.559 V (T3/T6) are used. When the input voltage is high (V_{IN} = 0.9 V), transistor T3 is turned on while T5 and T6 are turned OFF, which result in high output voltage (V_{OUT}= 0 V, logic 0) (Fig. 1.6(b)). In the same manner, when the input voltage is low (V_{IN}= 0 V), T6 is turned ON while T1 and T3 is turned OFF, which results in low output voltage (V_{OUT}= 0.9 V, logic 2). If the input voltage is intermediate (V_{IN}= 0.45 V), both T1 and T5 are turned ON while T3 and T6 are turn OFF, thus voltage dividing between saturation mode T2 and T4 makes intermediate (V_{OUT}= 0.45 V, logic 1).

However, when the saturation current of the ON-state CNTFET is used as the I_{CON}, a high P_S is consumed at intermediate state rather than the high and low states. In addition, the CNT diameter must be controlled to 0.5 nm (5 Å) to secure the V_T margin required for V_{DD} = 0.9 V operation, which is difficult to implement and large-scale integration. Moreover, there is a fundamental limitation of V_{DD} (> 0.6 V, with SSW= 60mV/dec and I_{ON}/I_{OFF}= 10^5) scaling due to multi-V_T (Fig. 1.6(c)).

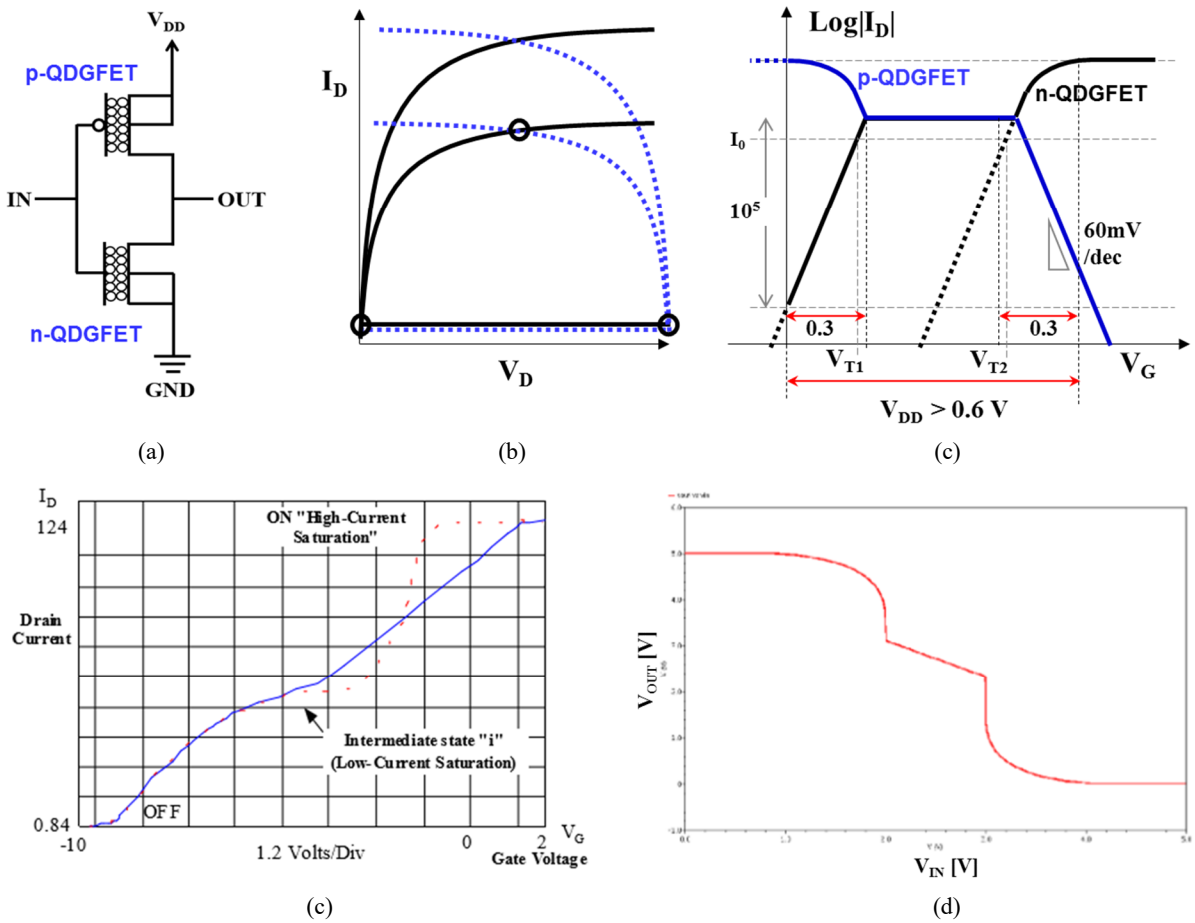


(a) (b) (c)

Figure 1.6. (a) CNTFET-based STI circuit [21] and (b) its I_{OUT}-V_{OUT} and (c) I_{OUT}-V_{IN} characteristics.

1.3.3 Ternary Device with Multi-V_T

To reduce the system complexity of multi-V_T-based ternary circuit, the researches about multi-V_T characteristics in single device have been reported. Recently, Intel has proposed a two-step *I-V* characteristic based on quantum dot (QDG) FET structure [22]-[24]. The I_{CON} is generated by coulomb blockade and resonant tunneling in the 2 layers of quantum dot (QD) of gate insulator region. Figure 1.7(a) shows the STI circuit configuration base on complementary *n/p*-type QDGFETs. Ideal QDGFET-based STI has identical *I-V* and voltage transfer characteristics with six CNTFET-based STI (Fig. 1.7(b)-(c)), however interference problem by QD scattering makes it difficult to realize V_G-independent I_{CON} and stable intermediate state (Fig. 1.7(d)-(e)) [24]. In addition, scaling of gate oxide thickness is not possible due to QD of a few nano-meter, and the P_S problems due to the I_{CON} in the ON state QDGFET and a P_D problems due to V_{DD} (> 0.6 V) scaling limit still remain.



(a) (b) (c)

(c) (d)

Figure 1.7. (a) CNTFET-based STI circuit and its ideal (b) I_{OUT}-V_{OUT} and (c) I_{OUT}-V_{IN} and fabricated (d) I_{OUT}-V_{OUT} characteristics and (e) VTC [24].

In [25], the multi-switching characteristics of the negative differential resistance (NDR) device used for STI circuits (Fig. 1.8(a)). The low and high states are formed at one crossing point by the first positive differential resistance (PDR) and OFF-state transistor, and by the second PDR and ON-state transistor, respectively (Fig. 1.8(b)). Whereas, three crossing points by NDR and ON-state transistor produce positive gain at intermediate state (Fig. 1.8(c)). The NDR device requires high $V_{DD} > E_g/q$ (= 2V, E_g is energy-band gap) for second NDR, and it is difficult to form a stable intermediate state and ternary circuit design due to non-monotonic I_D-V_D characteristics

Since the multi-V_T devices/circuits require V_{DD} increase, there is a fundamental limitation in designing and implementing ultra-low power MVL system.

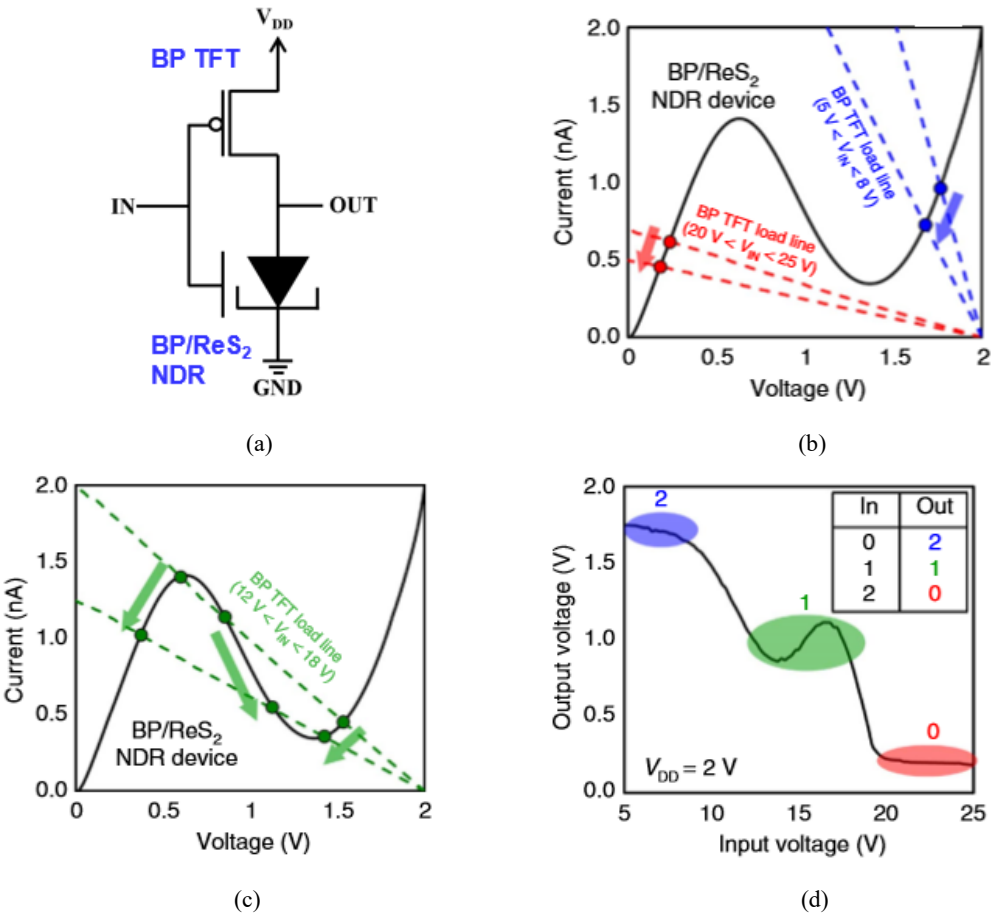


Figure 1.8. (a) NDR-based STI circuit and its I_{OUT}-V_{OUT} characteristics for (b) low, (c) intermediate, and (d) high-state transfer characteristics and (e) VTC [25].

1.4 Dissertation Outline

Based on the analysis of MVL research trends and problems, I propose a novel ternary device concept capable of V_{DD} scaling based on single-V_T and OFF-state constant leading ultra-low P_S and P_D. In Chapter 2, novel ternary device platform will be suggested and confirmed the logic change from binary to ternary based on CMOS technology using device simulation. In Chapter 3, the proposed Ternary CMOS (T-CMOS) is experimentally demonstrated and suggested T-CMOS design framework for ultra-low standby power **(**LSTP) operation. By developing the compact model of T-CMOS and verifying the physical model parameters with experimental data, compact T-CMOS STI operation is confirmed and discussed in terms of static noise margin (SNM) and OFF-leakage variation (OLV) from random-dopant fluctuation. In addition, advanced CMOS technology-based STI to improve SNM and V_{DD} scaling for ultra-low power operation is investigated. In Chapter 4, T-CMOS based MVL and multi-valued memory (MVM) applications are introduced and future work present in Chapter 5.

Chapter 2. Ternary Device Platform

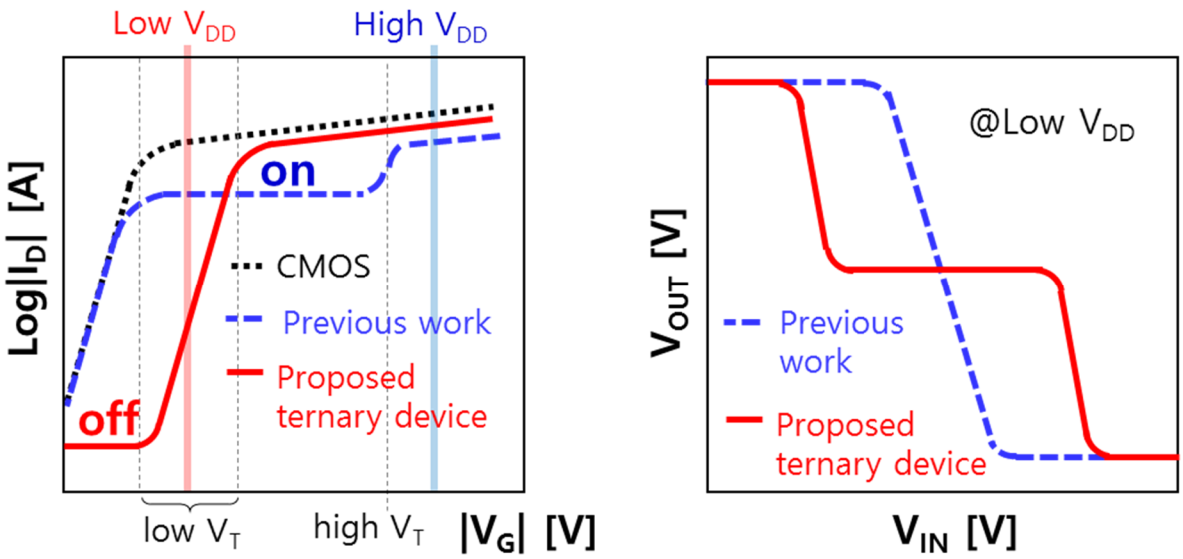
In this chapter, novel ternary device and its compact STI are proposed. The newly introduced *I-V* characteristics of proposed ternary device make possible to low P_S and P_D STI operation. To realize this low power compact STI, I study design methodology for the novel *I-V* characteristics with the conventional CMOS technology.

2.1 Novel Ternary Device Characteristics

As mentioned in Chapter 1, the previous ternary researches have designed a constant current in the ON-state, resulting in very high P_S at the intermediate state, and V_{DD} and P_D scaling were also impossible due to multi-V_T operation. Thus, I propose a new ternary device concept capable of V_{DD} scaling based on single-V_T and constant current in the OFF-state leading to ultra-low P_S and P_D operation.

2.1.1 Single Step I-V Characteristics

Figure 2.1(a) illustrates novel *I-V* characteristics of proposed ternary device compared with conventional binary CMOS and other previous work. **By designing the OFF-state constant current, not only the P_S issue of intermediate state is overcome, but single-step *I-V* characteristics are sufficient for ternary logic unlike the previous multi-step researches, so that continuous V_{DD} scaling and thus P_D scaling are possible**. The proposed ternary device operates as a low-power ternary device at low V_{DD} and high-performance binary device at high V_{DD}, whereas previous works operate as



(a) (b)

Figure 2.1. (a) Proposed single step log(I_{OUT})-V_{IN} characteristics with off-state constant current and (b) its low power STI operation with low V_{DD} compared with previous ternary research works.

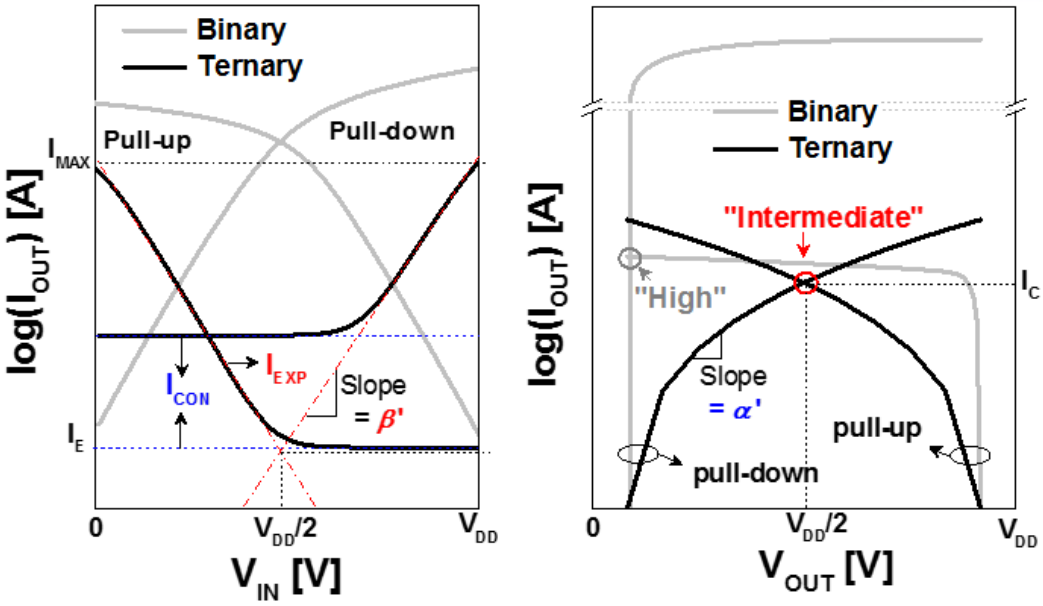


Figure 2.2. (a) Novel log(I_{OUT})-V_{IN} and log(I_{OUT})-V_{OUT} characteristics of complementary ternary device compared with conventional binary device.

high-power ternary device at high V_{DD} and low-performance binary device at low V_{DD} (Fig. 2.1(b)).

2.1.2 Simple Model of Ternary Device

As shown in Fig. 2.2, the newly introduced transfer I_{OUT}-V_{IN} and I_{OUT}-V_{OUT} characteristics are distinguished from conventional CMOS in that there are two bias-independent current mechanisms of the V_{IN}-independent (only V_{OUT}-dependent) constant current (I_{CON}) with I_C at V_{OUT}= V_{DD}/2 and V_{IN}-dependent (V_{OUT}-independent) exponential current (I_{EXP}) with I_{MAX} at V_{IN}= V_{DD} for pull-down or GND for pull-up (I_E @V_{IN}= V_{DD}/2) where $I_E < I_C < I_{MAX}$. It can be noted from Fig. 2.2 that the symmetric characteristics are applied in both complementary pull-up and pull-down elements for simplicity with the exponential V_{OUT}-dependence of I_{CON}. Therefore, novel complementary I-V characteristics for STI operation are expressed by following equations as [26]:

$$
\begin{aligned}
I_{OUT}(V_{IN}, V_{OUT}) &= I_{CON}(V_{OUT}) + I_{EXP}(V_{IN}) \\
I_{CON}(V_{OUT}) &= I_C exp[\pm \alpha(V_{OUT} - V_{DD}/2)] \\
I_{EXP}(V_{IN}) &= I_E exp[\pm \beta(V_{IN} - V_{DD}/2)]
\end{aligned}
\tag{2.1}
$$

where α and β are the exponent coefficient of each current mechanism and the signs of "+" and "-"in front of α and β are applied to pull-down and pull-up device, respectively. Here, I_{MAX}= $I_E$exp[β(V_{DD}/2)] is same in both pull-down and pull-up.

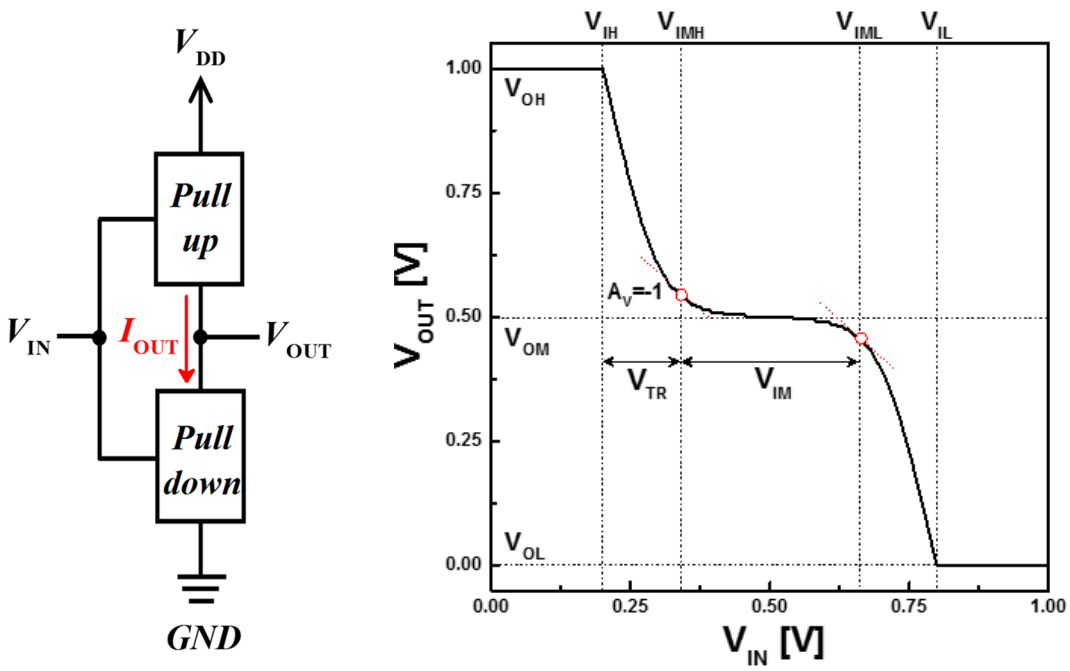
2.2 Standard Ternary Inverter (STI)

Compact STI is proposed based on the conventional binary inverter with a single V_{DD} by introducing novel *I-V* characteristics (Section 2.1.2) in each single pull-up and pull-down element.

2.2.1 Operation Principle and Voltage Transfer Characteristics

Figure 2.3 represents the calculation results of proposed compact STI VTC, which has three output states (V_{OH}= V_{DD}, V_{OM}= V_{DD}/2, V_{OL}= GND) according to four input regions (V_{IH}, V_{IMH}, V_{IML}, and V_{IL}). At here, for example case, α' (= α/ln(10))= 2 and β' (= β/ln(10))= 10 are used in Eq. (2.1) with I_{MAX}= 10^{-5} A and I_C= 10^{-8} A under V_{DD}= 1 V.

The operation principle of proposed STI can be explained with complementary I_{OUT}-V_{OUT} characteristics. Figure 2.4(a)-(c) show the tri-state voltage transfer procedure of low "0", intermediate "1", and high "2" output logic state, respectively, which are determined by the crossing points on complementary pull-up and pull-down I_{OUT}-V_{OUT} curves based on Eq. (1). **For low "0" or high "2" transition, pull-down or pull-up device shows one dominant current of I_{EXP} as I_{OUT} ~ I_{EXP} in V_{IN} > V_{IL} (Fig. 2.4(a)) or V_{IN} < V_{IH} (Fig. 2.4(c)), and thus, current path is created to GND (V_{OL}) or V_{DD} (V_{OH}), respectively. During V_{OUT} transition to V_{DD}/2 around V_{IMH} and V_{IML}, both are comparable as I_{OUT}= I_{CON} + I_{EXP}, which can lead to slow transition.** Finally, the additional intermediate "1" state



(a) (b)

Figure 2.3. Calculation results of the proposed STI VTC. For example case here, α'= 2 and β'= 10 are used in Eq. (1) with I_{MAX}= 10^{-5} A and I_C= 10^{-8} A under V_{DD}= 1 V.

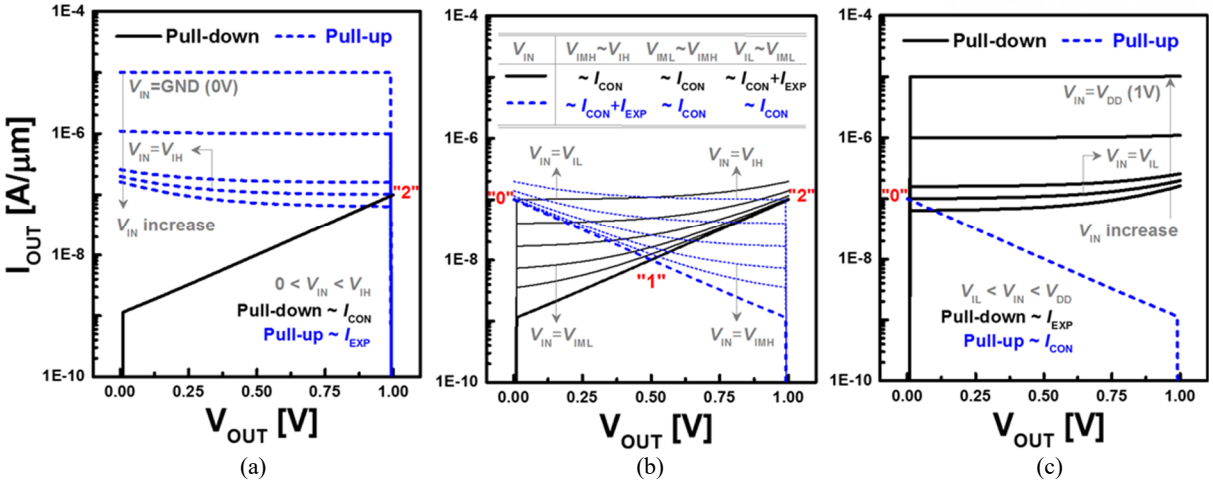


Figure 2.4. Calculation results of the proposed I_{OUT}-V_{OUT} characteristics of pull-up and pull-down device for (a) high-state (marked "2") transfer at low input voltage ($V_{IN} \leq V_{IH}$), (b) "intermediate"-state (marked "1") transfer at $V_{IMH} \leq V_{IN} \leq V_{IML}$, and (c) low-state (marked "0") transfer at high input voltage ($V_{IN} \geq V_{IL}$).

(V_{OM}) is obtained by one crossing point at $V_{OUT} = V_{DD}/2$ in $V_{IMH} < V_{IN} < V_{IML}$ where I_{OUT} of the pull-up and pull-down is dominated by only I_{CON} (Fig. 2.4(b)).

2.2.2 Analysis of Operation Conditions

For STI operation, the conditions of four input voltages $V_{IL} < V_{DD}$, $V_{IML} > V_{DD}/2$, $V_{IMH} < V_{DD}/2$, and $V_{IH} > 0$(= GND) should be valid. These four input voltages are determined by complementary combination of pull-down and pull-up current equation.

For $V_{IN} = V_{IH}$, $\{I_{CON}\}_{\text{pull-up}} = \{I_{EXP}\}_{\text{pull-down}}$ with $V_{OUT} = V_{DD}$ as:

$$V_{IH} = \frac{1}{\beta} ln\left(\frac{I_{MAX}}{I_C}\right) - \frac{\alpha}{\beta}\frac{V_{DD}}{2} \tag{2.2}$$

For $V_{IN} = V_{IMH}$, $dV_{OUT}/dV_{IN} = -1$ from the $\{I_{CON} + I_{EXP}\}_{\text{pull-up}} = \{I_{EXP}\}_{\text{pull-down}}$ with $V_{OUT} = V_{DD}$ as:

$$V_{IMH} = \frac{1}{\beta} ln\left(\frac{I_{MAX}}{I_C}\right) + \frac{1}{\beta} ln\left(\frac{\beta}{2\alpha}\right) \tag{2.3}$$

For $V_{IN} = V_{IMH}$, $dV_{OUT}/dV_{IN} = -1$ from the $\{I_{EXP}\}_{\text{pull-up}} = \{I_{CON} + I_{EXP}\}_{\text{pull-down}}$ with $V_{OUT} = V_{DD}$ as:

$$V_{IML} = V_{DD} - \frac{1}{\beta} ln\left(\frac{I_{MAX}}{I_C}\right) - \frac{1}{\beta} ln\left(\frac{\beta}{2\alpha}\right) \tag{2.4}$$

For V_{IN}= V_{IH}, $\{I_{EXP}\}_{pull\text{-}up}$= $\{I_{CON}\}_{pull\text{-}down}$ with V_{OUT}= V_{DD} as:

$$V_{IL} = V_{DD} - \frac{1}{\beta} ln\left(\frac{I_{MAX}}{I_C}\right) + \frac{\alpha}{\beta}\frac{V_{DD}}{2} \tag{2.5}$$

The intermediate V_{IN} range is defined as V_{IM}= V_{IML}-V_{IMH}:

$$V_{IM} = V_{DD} - \frac{2}{\beta} ln\left(\frac{I_{MAX}}{I_C}\right) - \frac{2}{\beta} ln\left(\frac{\beta}{2\alpha}\right) \tag{2.6}$$

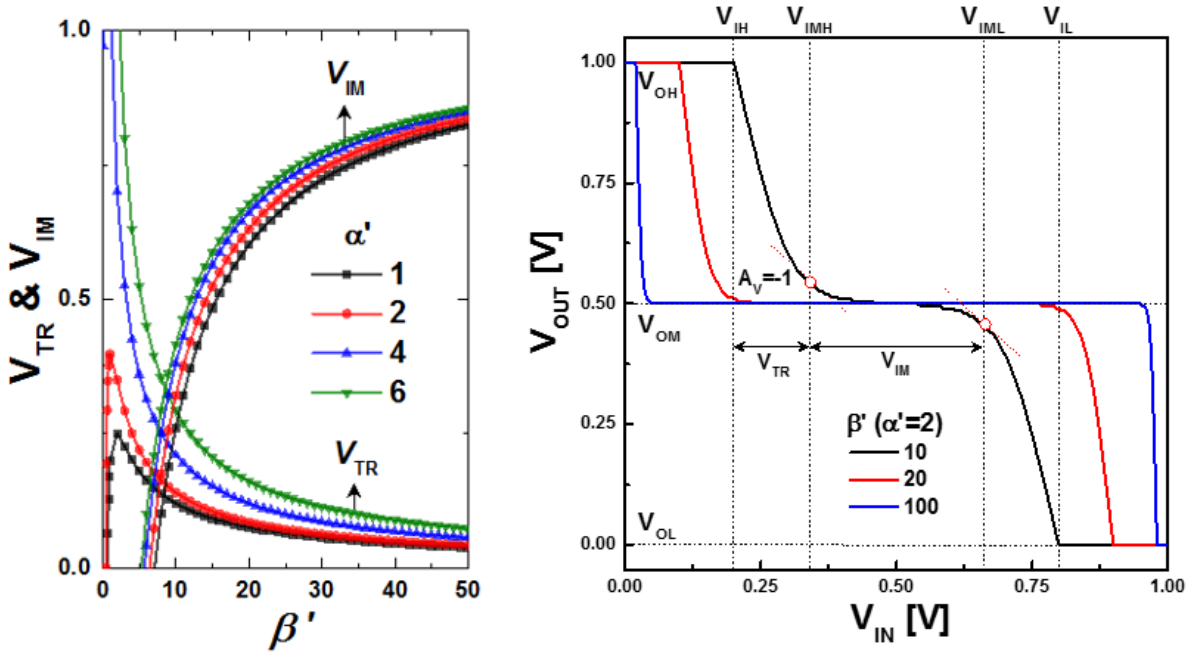
The transition voltages are defined as V_{TR}= V_{IMH}-V_{IH}= V_{IL}-V_{IML}:

$$V_{TR} = \frac{\alpha}{\beta}\frac{V_{DD}}{2} + \frac{1}{\beta} ln\left(\frac{\beta}{2\alpha}\right) \tag{2.7}$$

From the V_{IL} < V_{DD}, V_{IML} > V_{DD}/2, V_{IMH} < V_{DD}/2, and V_{IH} > 0(= GND) for STI operation, criterion for α' and β' derived as:

$$\alpha' = \frac{\alpha}{ln(10)} < log\left(\frac{I_{MAX}}{I_C}\right) \Big/ \frac{V_{DD}}{2} << \beta' = \frac{\beta}{ln(10)} \tag{2.8}$$

As shown in Fig. 2.5(a), under the ranges of α' and β'given by Eq. (2.8), the lower V_{TR} and the higher V_{IM}, which are preferable for ideal STI VTC, can be obtained by the larger β'and smaller α' but both have a certain saturated value owing to the term of log(β'/2α')/β' in Eq. (2.6) and (2.7). This nonlinear log(x)/x function in terms of β' is derived only at V_{IMH} and V_{IML} near V_{DD}/2 where either pull-up or pull-down current has the nonlinear I_{OUT} = I_{CON} + I_{EXP} with comparable I_{CON} and I_{EXP}. Even though the larger β' as much as possible looks preferable only considering the smaller V_{TR}, however, it is expected that there would be an optimum for β' for a reasonable V_{IM} considering the noise margins (Fig. 2.5(b)), which will be discussed in Section III.



(a) (b)

Figure 2.5. Calculation results of (a) V_{TR} and V_{IM} and (b) VTCs of STI with a wide range of α' and β' at V_{DD}= 1V. At here $\log(I_{MAX}/I_C)/(V_{DD}/2)$ set as 6.

2.3 Design Methodology of CMOS for STI Operation

To realize this compact STI, I investigate the design methodology for the novel *I-V* characteristics with conventional CMOS technology. The V_{IN}-independent I_{CON} as an essential current mechanism for additional intermediate "1" state of STI can be implemented with a gate bias-independent junction band-to-band tunneling (BTBT) current (I_{BTBT}) in the nanoscale CMOS, which also provides a gate bias-dependent I_{EXP} by subthreshold current (I_{sub}) for high "2" and low "0" state.

Based on the basic structural information from LSTP 32 nm technology in ITRS [27], conventional MOSFET is calibrated by having the experimental on/OFF-current range of 32 nm HK/MG CMOS characteristics [28] with equivalent oxide thickness (EOT) of 1 nm, highly (HDD) and lightly doped drain (LDD) doping concentration of N_{HDD}= 1×10^{20} cm^{-3} and N_{LDD}= 2.5×10^{19} cm^{-3}, respectively. Figure 2.6 and Table 1 summarize the calibration process of 32nm HK/MG CMOS. On this channel doping of 2×10^{18} cm^{-3} for conventional CMOS, dominant I_{OFF} (@V_{GS}= 0V) is the I_{sub} based on the normal drift-diffusion transport. Device simulation was performed by Synopsys *Sentaurus*™ with nonlocal BTBT model including band-gap narrowing [29].

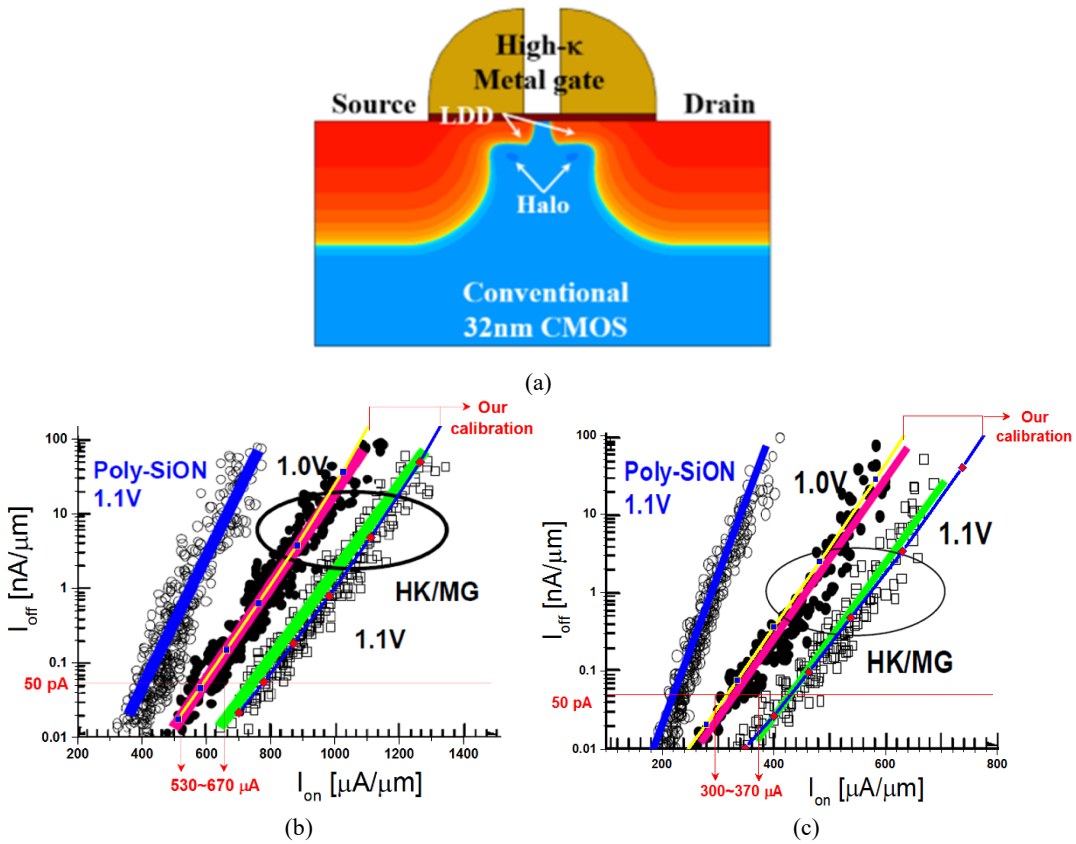


Figure 2.6. (a) Structure of planar 32 nm HK/MG CMOS and (b) *n*MOS and (c) *p*MOS calibration results with experimental HK/MG data [28].

Table 2.1. Low standby power 32 nm technology calibration

LSTP 32 nm technology	This work		ITRS [27]	Ref. [28]	
	*n*MOS	*p*MOS	*n*MOS	*n*MOS	*p*MOS
L_G [*nm*]	32		32	30	
EOT [*nm*]	1		1	Unknown	
N_{ch} [cm^{-3}]	2×10^{18}		3.7×10^{18}	Unknown	
V_{DD} [*V*]	1		1.05	1	
I_{OFF} [$pA/\mu m$]	50	50	50	50	50
I_{ON} [$\mu A/\mu m$]	590	320	559	530~670	300~370

2.3.1 OFF-State Band-to-Band Tunneling Mechanism

Figure 2.7 shows the two-dimensional (2D) cross-section view of 32 nm high-k/metal-gate (HK/MG) planar *n*MOS with simulated BTBT generation rates for the calibrated conventionally-low and intentionally-high channel doping concentration (N_{ch}) of 2×10^{18} cm^{-3} and 2×10^{19} cm^{-3}, respectively. **Only by increasing N_{ch} on the default Kane's BTBT model parameters, the maximum BTBT location has been shifted from a gate-overlapped LDD region (left inset) to a HDD-to-body junction (right inset), which results in the dominant OFF-state current mechanism of V_G-independent I_{BTBT}.**

Figure 2.8 demonstrates that the calibrated I_D-V_G curves for 32 nm CMOS devices [27]-[28] become the newly-introduced I_D-V_G curves for STI (cf. Fig. 2.2) according to N_{ch} increase on symmetrically designed *n*/*p*MOS. Typical N_{ch} for STI is determined as 2×10^{19} cm^{-3} since it allows I_{BTBT}~ 50 pA/μm for

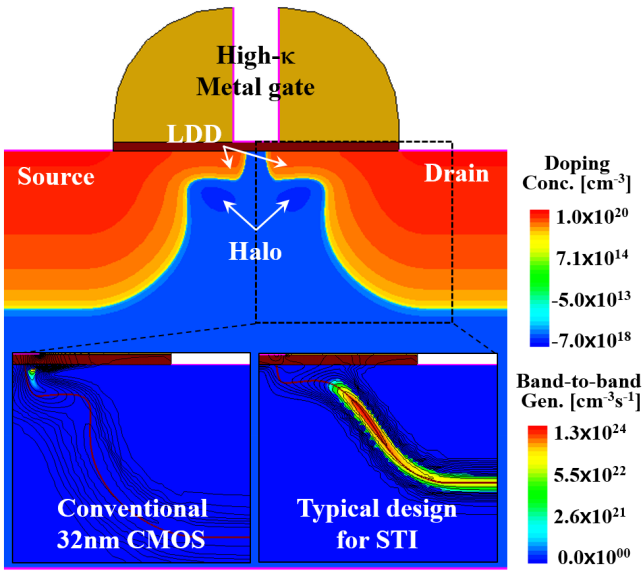


Figure 2.7. Structure of planar 32nm CMOS with BTBT generation view at different N_{ch} of 2×10^{18} cm^{-3} and 2×10^{19} cm^{-3}.

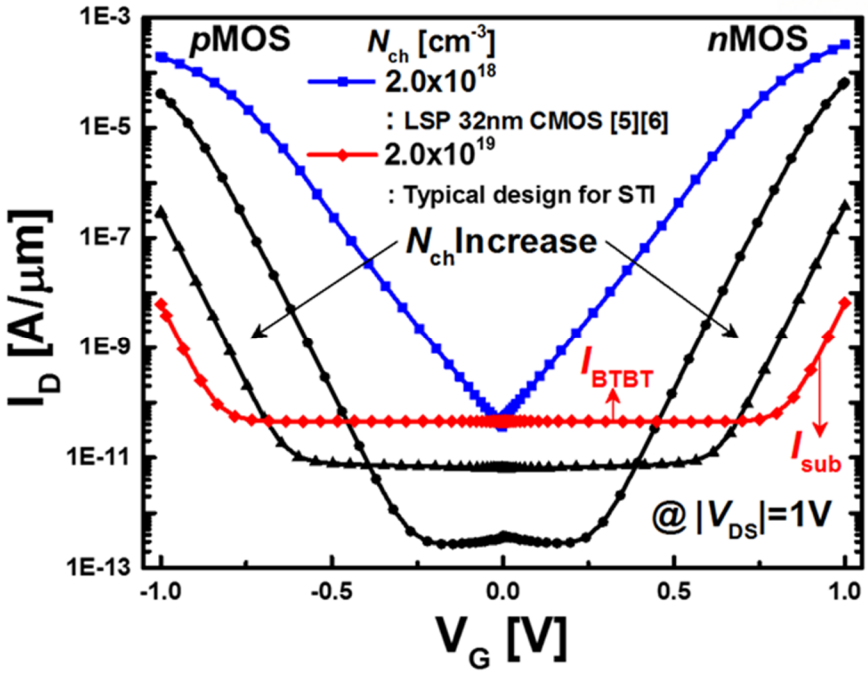


Figure 2.8. Simulated transfer I_D–V_G characteristics of symmetric planar *n*/*p*MOS. Only increasing N_{ch} from 2×10^{18} cm^{-3} and 2×10^{19} cm^{-3}, novel ternary CMOS operation could be obtained.

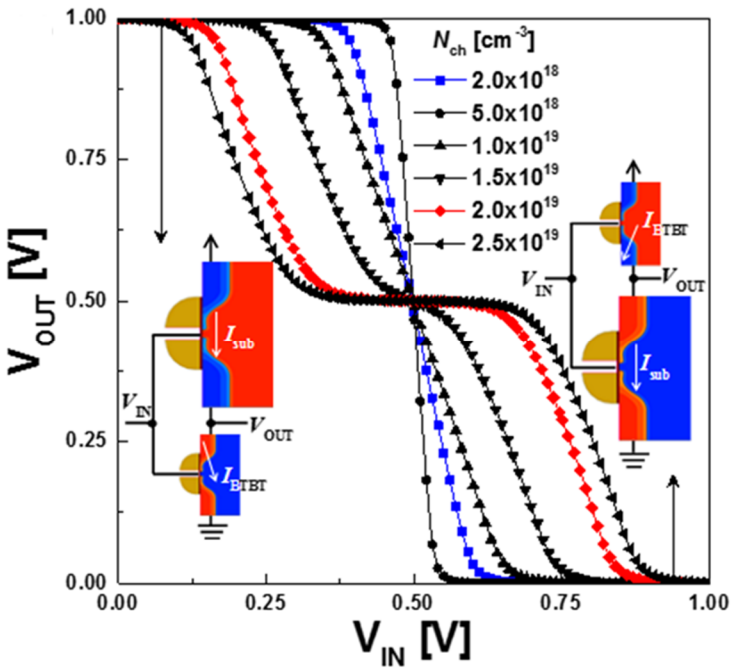


Figure 2.9. Mixed-mode device simulation results of inverter VTCs with various N_{ch}. Logic gate of CMOS inverter changes from binary to ternary at high N_{ch}.

planar CMOS as the same OFF-current (I_{OFF} @V_G= 0 V) with the calibrated LSTP 32 nm CMOS.

2.3.2 Logic Changes from Binary to Ternary with Channel Conditions

As shown in Fig. 2.9, mixed-mode device simulation confirms that the **logic gate of CMOS**

inverter changes from binary to ternary only by increasing N_{ch} and STI operation can be demonstrated based on OFF-state current mechanisms of I_{BTBT} and I_{sub} by using conventional planar nano-CMOS technology. Therefore, a CMOS design capable of ternary operation is called Ternary CMOS (T-CMOS) by differentiating it from conventional CMOS. It should be noted that other PTI and NTI functions can be implemented by using only highly doped ternary *n*MOS (T-*n*MOS) (e.g. N_{ch}= 2×10^{19} cm^{-3}) with conventional *p*MOS (e.g. N_{ch}= 2×10^{18} cm^{-3}) for PTI (Fig. 2.10(a)) and only highly doped ternary *p*MOS (T-*p*MOS) (e.g. N_{ch}= 2×10^{19} cm^{-3}) with conventional *n*MOS (e.g. N_{ch}= $2\times10^{18}cm^{-3}$) for NTI (Fig. 2.10(b)) in our compact CMOS inverter architecture, respectively. The core of the T-CMOS researches is the realization of fully V_G-independent I_{BTBT}, so it will be discussed in Chapter 3.

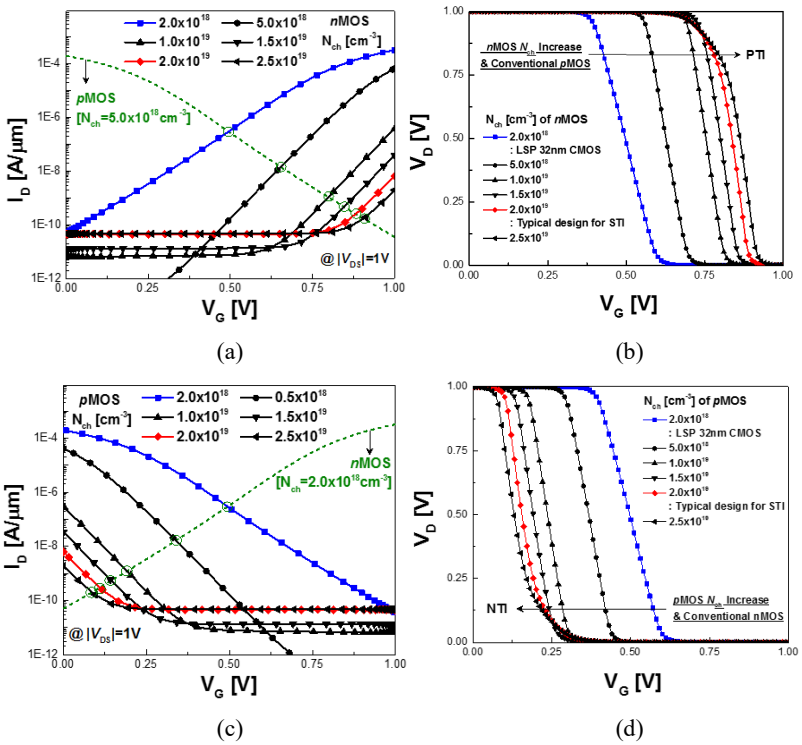


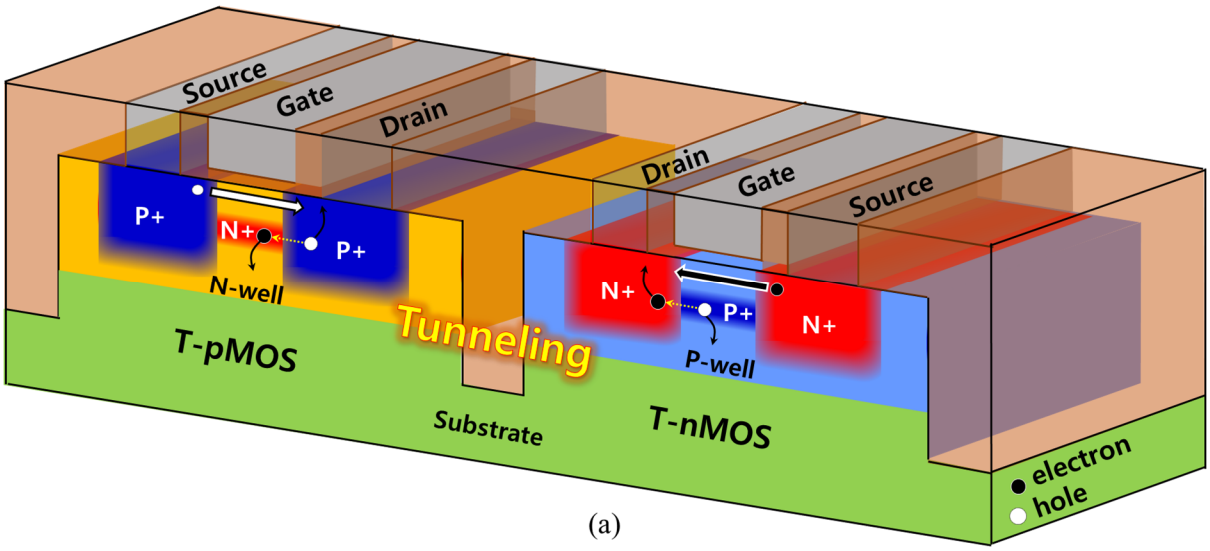
Figure 2.10. (a) I_D-V_G characteristics of highly doped *n*MOS and conventional *p*MOS for PTI and (b) its voltage transfer curves. (c) I_D-V_G characteristics of highly doped *p*MOS and conventional *n*MOS for PTI and (d) its voltage transfer curves.

Chapter 3. Experimental Demonstration of Ternary CMOS (T-CMOS)

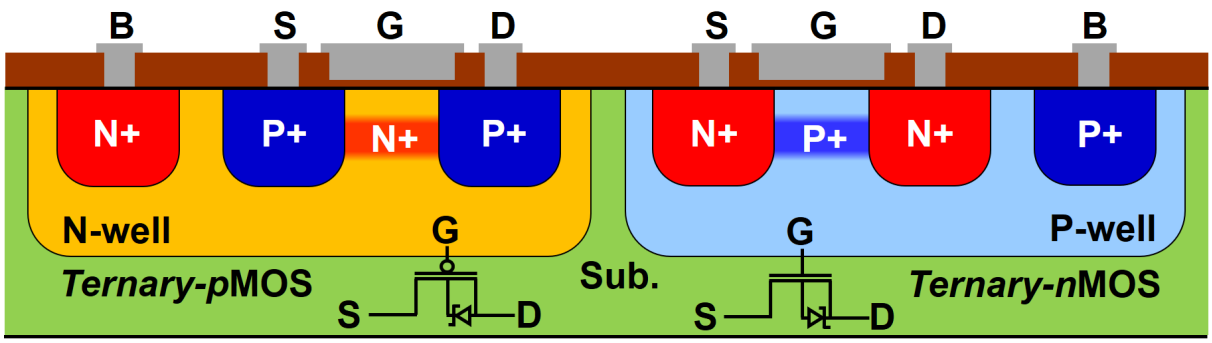
In this chapter, the feasible and scalable T-CMOS with a single-V_T is demonstrated for the first time and develop its compact model for fully CMOS-compatible physical synthesis of ternary circuit. Based on verified T-CMOS compact model, low power STI operation will be confirmed and discussed in terms of static noise margin (SNM) and OFF-leakage variation (OLV) from random-dopant fluctuation. In addition, performance enhancement of STI will be investigated base on various advanced CMOS structure including ternary FinFET (T-FinFET). Moreover, V_{DD} scaling will be studied for ultra-low static and dynamic power applications.

3.1 Experimental Design of T-CMOS

Figure 3.1 illustrates the three-dimensional (3D) bird's eyes view and 2D cross sectional view of



(a)



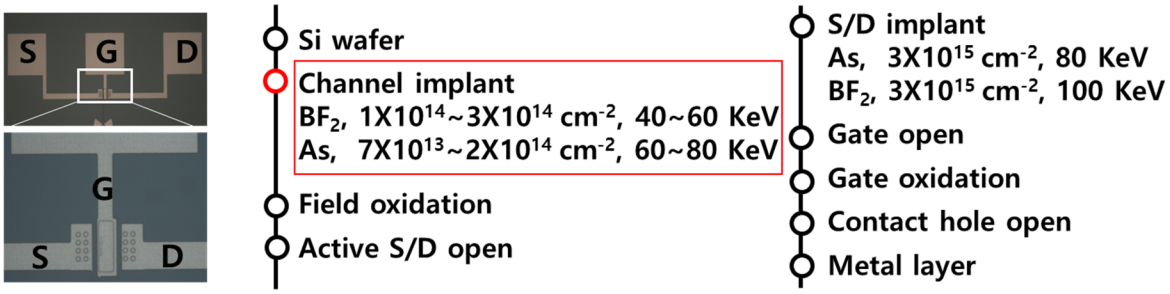
(b)

Figure 3.1. T-CMOS structure in (a) 3D bird's eye view with carrier injection mechanism and (b) 2D cross-sectional view with device symbol.

proposed T-CMOS. Especially, T-CMOS has the same structure and process with conventional CMOS except for heavily doped *pn* junction under the channel region. By placing a channel-to-drain junction away from the gate, completely V_G-independent BTBT current can be obtained. Based on carrier injection mechanism, T-CMOS symbols are combined with CMOS and zener diode symbols.

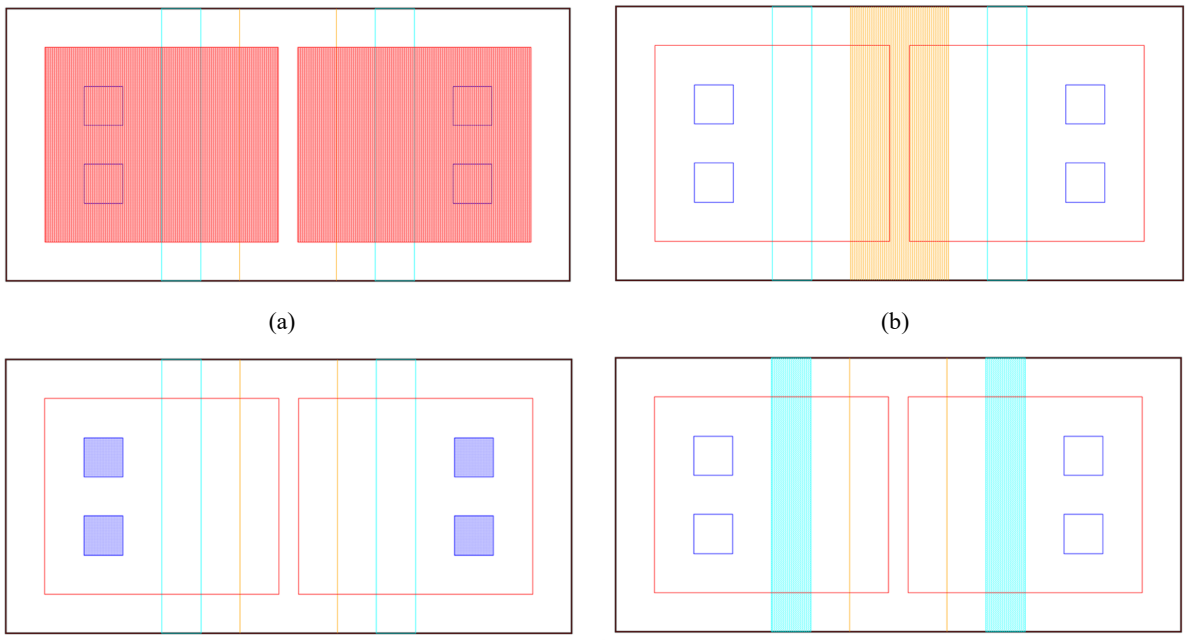
3.1.1. Device Fabrication

Figure 3.2(a) presents a top-view micrograph image of the fabricated T-CMOS by fully CMOS-compatible fabrication process (Fig. 3.2(b)) [30]. At here, four make layers are used for T-CMOS fabrication: the first active layer for source and drain doping (Fig. 3.3(a)), the second gate open layer



(a) (b)

Figure 3.2. (a)Top view micrograph image and (b) process flow of T-CMOS: only increased channel dose and energy in conventional gate-last CMOS process.



(a) (b)

(c) (d)

Figure 3.3. Four make layer used in T-CMOS: (a) active layer for source and drain doping, (b) gate open layer for a well-grown gate oxide, (c) contact layer for via hole contact between metal and source/drain, (d) fourth metal layer for metal separation of gate, source, and drain.

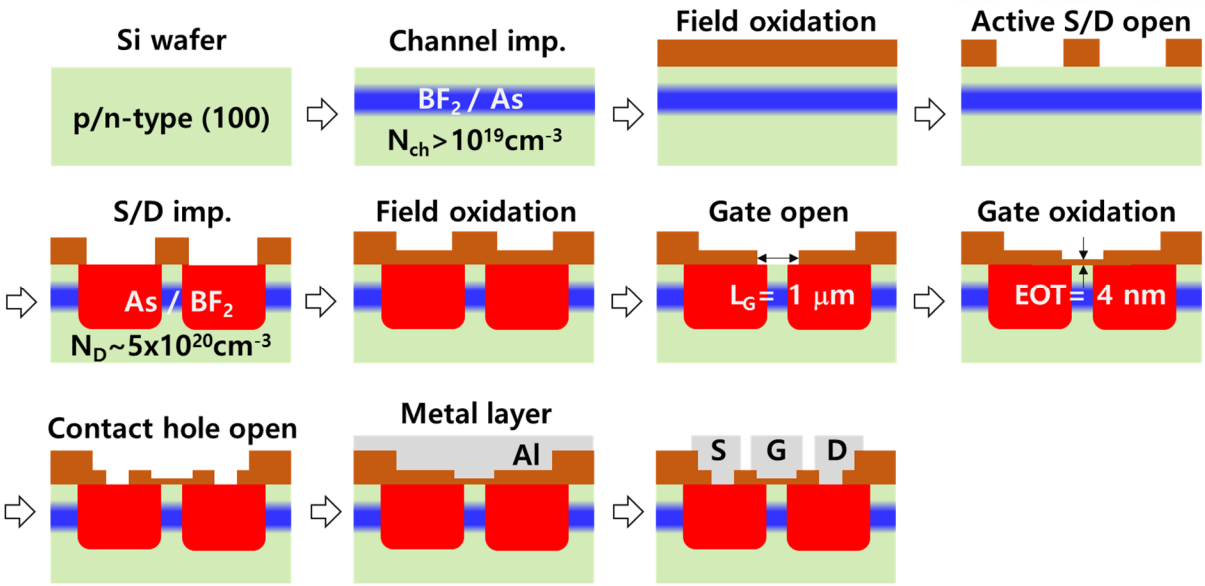


Figure 3.4. T-CMOS fabrication process: only increased channel dose and energy in conventional gate-last CMOS process.

for a well-grown gate oxide (Fig. 3.3(b)), the third contact layer for via hole contact between metal and source/drain (Fig. 3.3(c)), and the fourth metal layer for metal separation of gate, source, and drain (Fig. 3.3(d)). Ternary *n*/*p*MOS (T-*n*/*p*MOS) devices were respectively fabricated on *p*/*n*-type Si (100) wafer with physical gate length (L_G) of 1 μm, gate width (W) of 28 μm equivalent oxide thickness (EOT) of 5 nm based on gate-last CMOS process, which are summarizes in Fig. 3.4. At first, **to implement the fully V_G-independent I_{BTBT}, channel was implanted BF_2 and As for T-*n*/*p*MOS with intentionally high dose over 10^{14} cm^{-2} and energy of 40~60 and 60~80 keV for N_{ch} > $1x10^{19}cm^{-3}$.** Field oxide of 2000 Å was deposited using plasma-enhanced chemical vapor deposition (PECVD) and then densified at 700C ºC for 30min. Through the first photolithography step with active layer mask, the L_G and source/drain regions could be defined, and then the field oxide on source/drain regions was removed with dry etching process in CHF_3/CF_4 reactive ion plasma. Source and drain were deeply implanted with As and BF_2 for T-*n*/*p*MOS with dose of $3x10^{15}$ cm^{-2} and energy of 80 and 100keV, respectively. Subsequently, the inter-layer dielectric (ILD) oxide of 2000 Å was deposited using PECVD and densified at 700C ºC for 30min, once more. Applying second photolithography step with gate open layer mask, passive oxide on gate-channel coupling region was removed with wet cleaning. After that, the gate oxide was grown for 30 min in two types: a high temperature of 950 ºC and a low temperature of 800 ºC to analyze the high and low thermal budgets. The third photolithography with contact layer mask and wet cleaning processes are performed for via hole contact between metal and source/drain. Finally, aluminum (including 1% Si) was deposited by dc sputtering and isolated for gate, drain, and source.

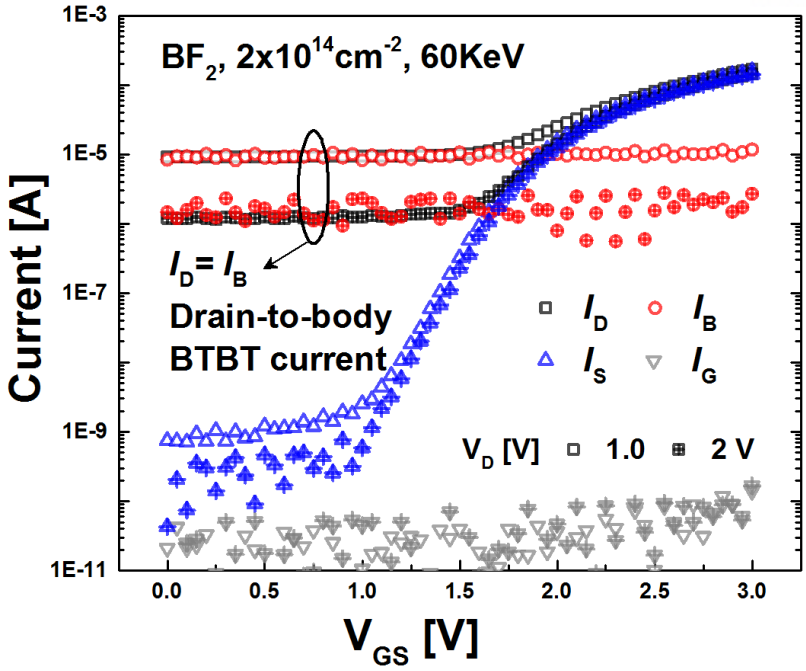


Figure 3.5. (a) Measured I_D-V_G and of the fabricated T-*n*MOS, which has V_G-independent off-state current (I_D= I_B @ V_{GS} < V_T) and V_G exponentially dependent I_{MAX} (= I_S).

Figure 3.5 shows the measured I_D-V_G characteristics of fabricated T-*n*MOS (channel condition: BF_2, 2×10^{-14} cm^{-2}, 60keV), which has V_G-independent (only V_D-dependent) junction BTBT (drain-to-body current, I_D= I_B) at OFF-state and V_G-exponentially dependent (V_{OUT}-independent) I_{sub} (I_D= I_S) with high V_T= 2 V. Fabricated T-*n*MOS satisfied STI operation condition of Eq. (2.8) with extracted α' (= 0.77) < log (I_{MAX}/I_C)/(V_{DD}/2) (=1.61) < β'(= 4.89) at V_{DD}= 2.4 V.

3.1.2. Experimental Results and Discussion

Figure 3.6 (a) shows the measured I_D-V_G characteristics of the fabricated T-CMOS compared with *n*MOS, which are designed based on the simulated channel doping profile of Fig. 3.6(b) reflecting the process. The two groups of [i]-[iii] and [iv]-[vi] have a dry oxidation process at 950 ºC and 800 ºC for 30 min respectively, and both groups have the same subsequent thermal processes of rapid thermal annealing (RTA) at 1000 ºC for 10 sec and two-times field oxidations at 700 ºC for 30 min under different dose amounts. The [i] and [ii] represent the conventional *n*MOS characteristics with the OFF-current of I_{sub} and the gate-induced drain leakage (GIDL) respectively, since the peak channel doping concentrations (C_P) less than 1×10^{19} cm^{-3} are predicted. On the other hand, the [iii]-[vi] with $C_P > 1\times10^{19}$ cm^{-3} indicate T-*n*MOS characteristics with OFF-current of fully V_G-independent I_{BTBT} and its levels are determined by C_P. At here, the symmetric BTBT current density (J_{BTBT}) of T-*n/p*MOS can be obtained by designing C_P based on the proven ion implantation process owing to same tunneling mass of electron

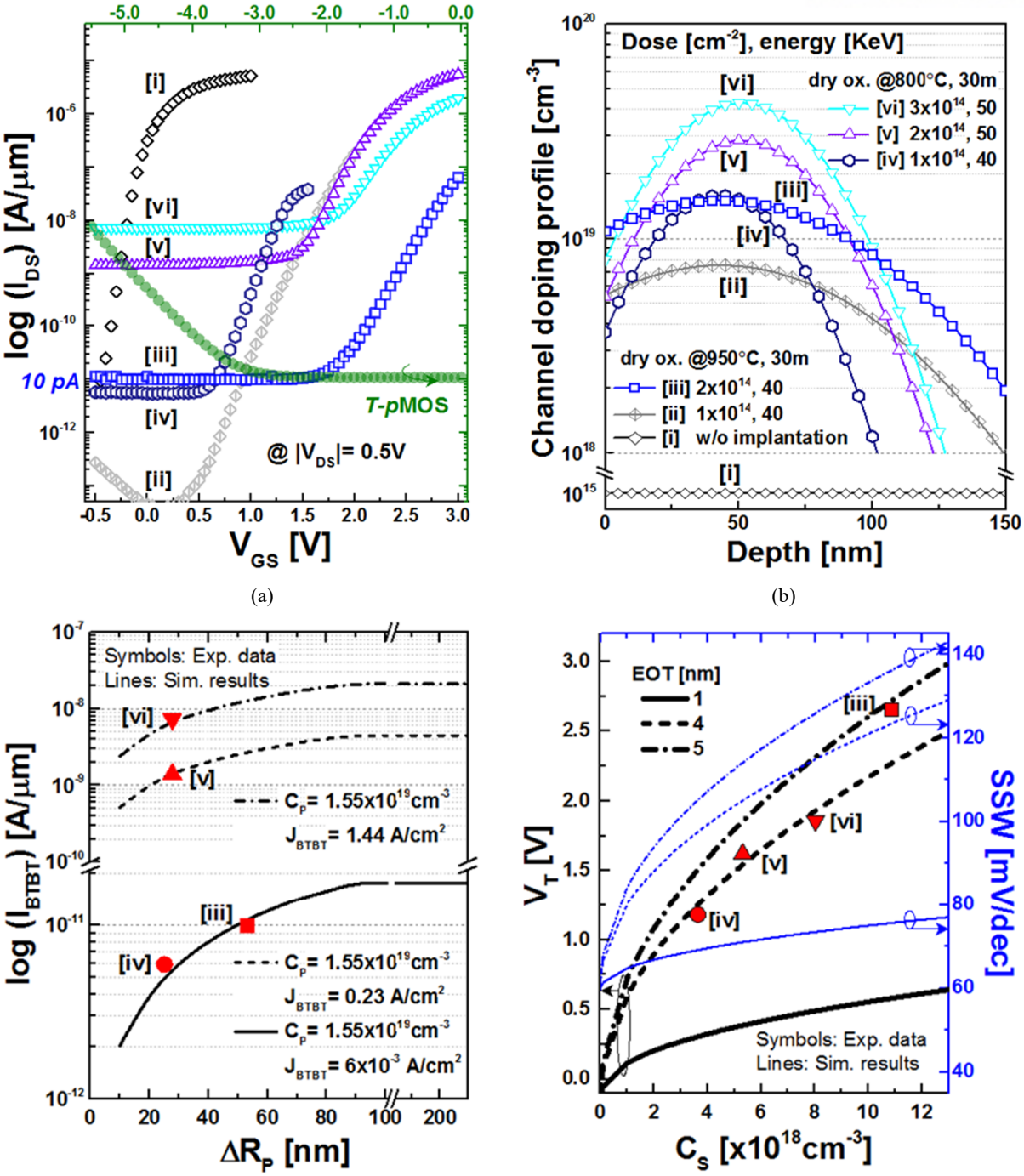


Figure 3.6. (a) Measured I_D-V_G characteristics of fabricated T-*n*/*p*MOS and *n*MOS and (b) its simulated channel doping profiles reflecting the process. (c) Simulated I_{BTBT} according to ΔR_P and C_P and (d) V_T and SSW according to C_S.

and hole. The T-*n*MOS of [iii] and [iv] and T-*p*MOS were designed with J_{BTBT} = 6×10^{-3}A/cm^2 at V_D= 0.5 V based on the same C_P = 1.55×10^{19} cm^{-2}, and I_{BTBT} difference between [iii] and [iv] at the level of several *p*A/μm is proportional to the junction area (Area= W × 0.8ΔR_P, where ΔR_P is standard deviation) as shown in Fig. 3.6(c). The small ΔR_P for low I_{BTBT} can be implemented through a low thermal budget,

which also reduces the surface doping concentration (C_S). This C_S is a key design parameter controlling the I_{sub} characteristic with V_T and SSW, and all the experimental data of [i]-[vi] follows the tendency that low C_S has low V_T as shown in Fig. 3.6(d). In particular, the [iii] and [iv] are designed with same C_P and different C_S, and a significantly large V_T difference was measured at 2.66 and 1.18 V compared to small I_{BTBT} difference of 11.4 and 5.7 $pA/\mu m$. In addition, gate controllability can be improved by EOT scaling of 1 nm, which results in excellent T-CMOS characteristics with $V_T < 0.5$ V and SSW ~ 70 mV/dec. **Therefore, by forming a low-high channel profile through low-thermal budget, the BTBT and subthreshold diffusion mechanisms can be independently controlled and I_{BTBT} and I_{sub} are improved respectively with design parameters such as C_P, junction area, C_S and EOT**.

Figure 3.7 and 3.8 analyze the retrograde (low-high) channel more specifically. At here, exponential coefficient of α' and β' for V_{IN}-independent I_{CON} and V_{IN}-exponentially dependent I_{EXP} of Eq. (2.1) apply identically to similar type of I_{BTBT} and I_{sub}. Based on various retrograde channel profiles of T-CMOS designed with C_P, projection rage (R_P) and, ΔR_P (= 0.0606×R_P) of Fig. 3.7, the key parameters α' and β' are investigated in Fig. 3.8. When the R_P was designed far away the interface more than 0.2 μm with fixed ΔR_P of 30 nm, the β' are saturated at the maximum values of $2.3(kT)/q\ln(1+C_{dm}(N_{sub})/C_i(EOT))$ with constant N_{sub} (= C_S) = $1\times10^{17}cm^{-3}$ thus, second variable EOT and C_P only effect on β' and α' respectively (Fig. 3.8 (a) and (b)). As same way, when the $\Delta R_p < 50$ nm with fixed R_p of 0.3 μm, the α' and β'can be independently controlled with EOT and C_P as shown in Fig. 3.8(c) and (d).

Figure 3.9 shows the I_D-V_G characteristics of *T-n/p*MOS according to EOT scaling. Comparing measured I_D-V_G curves of *T-n*MOS with EOT= 5nm (dry oxidation at 800 ºC for 30 min) and 10 nm (at

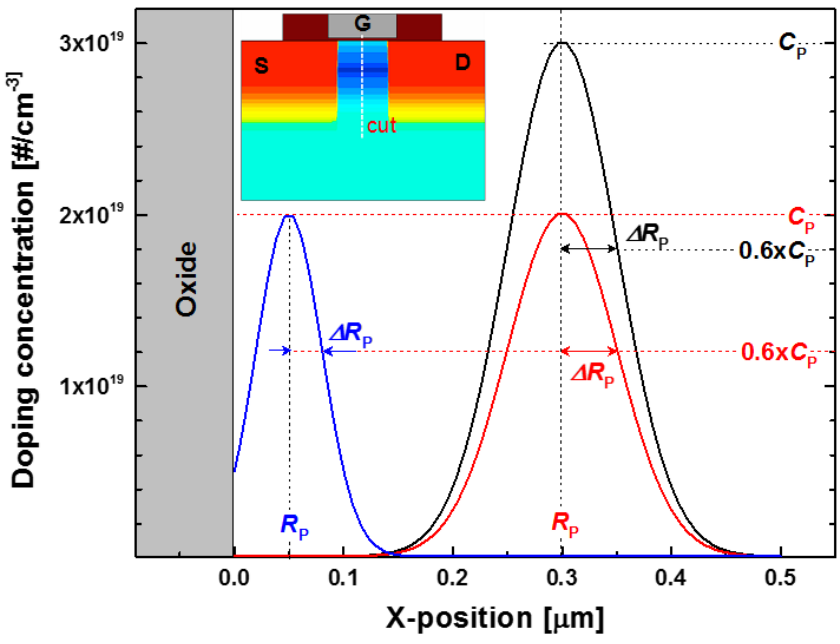


Figure 3.7. Retrograde (low-high) channel profile of T-CMOS with various C_P, R_P, and ΔR_P.

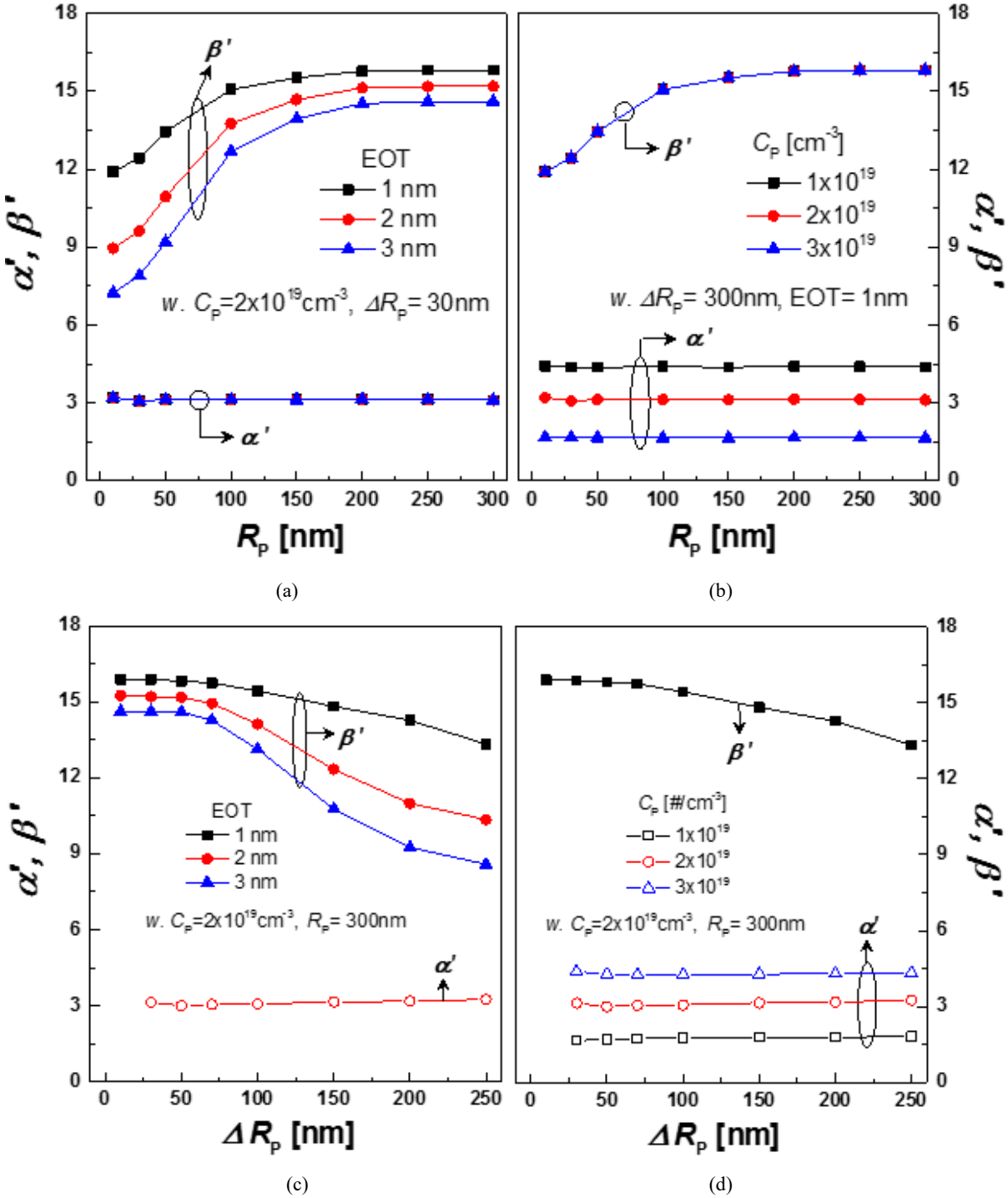
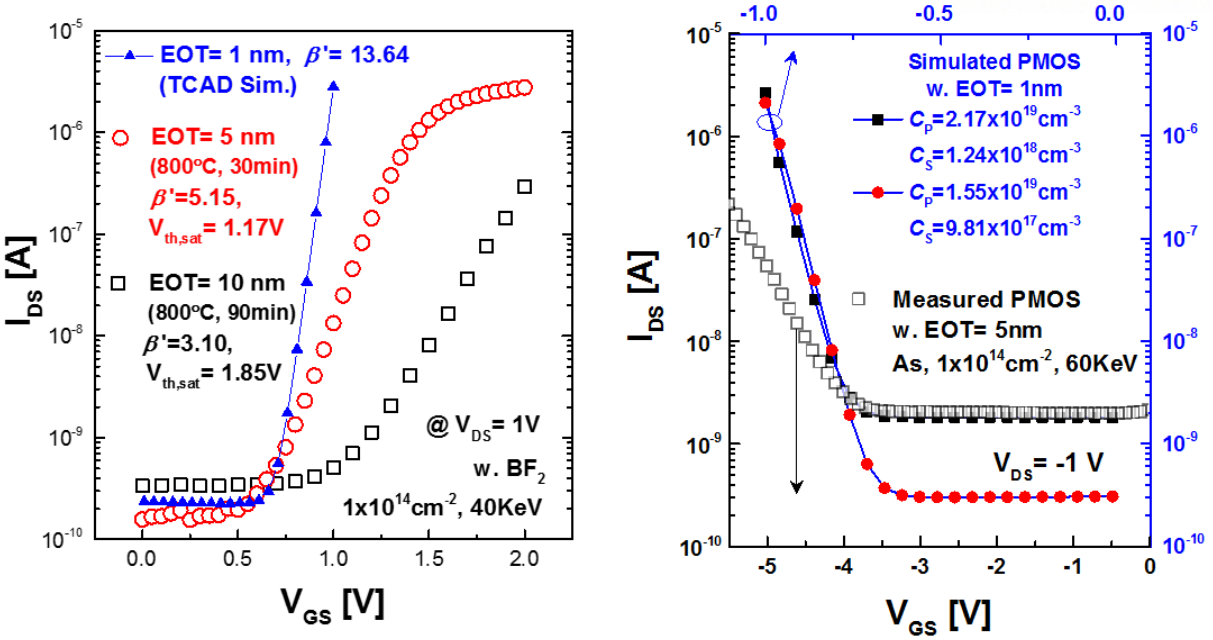


Figure 3.8. The α' and β' as function of ΔR_P with second variable of (a) EOT and (b) C_P, and ΔR_P with second variable of (c) EOT and (d) C_P.

800 ºC for 90 min) under the same implant condition (dose= 1×10^{14}cm^{-2}, 60 keV), the β' increased from 3.1 to 5.15 and V_T decreased from 1.85 V to 1.17 V in Fig. 9(a). In addition, simulated results of EOT= 1 nm shows the β' enhancement up to 13.64 (SSW= 74 mV/dec), which is possible to STI operation with V_{DD}= 1 V. At here, the V_T of simulated T-*n*/*p*MOS are adjusted with metal work-function for better



(a) (b)

Figure 3.9. The I_D-V_D characteristics of (a) T-*n*MOS and (b) T-*p*MOS with EOT= 1 nm (simulated data), 5 nm, and 10 nm (experimental data).

SSW comparison. In the same methodology, *T-p*MOS can be operated below 1 V with EOT scaling as shown in Fig. 3.9(b).

3.1.3. T-CMOS design framework

Figure 3.10 represents T-CMOS design framework by plotting I_{MAX} (I_{sub} @V_{DD})-I_C (I_{BTBT} @V_{DD}/2) curves with a single-V_T according to N_{ch}, which corresponds to the robust I_{OFF}-I_{ON} curves of conventional binary CMOS design. At here, L_G= 32 nm, W= 100 nm, and EOT= 1 nm are used for device simulation. In the $N_{ch} < 1\times10^{19}$cm^{-3}, conventional binary CMOS operation is observed and I_{ON} and I_{OFF} determine high performance and low standby power operation, respectively. On the other hand, in the $N_{ch} > 1\times10^{19}$cm^{-3}, a novel T-CMOS operation is obtained, and I_{MAX} determines the performance of high and low states and I_C decides the performance of intermediate state and low standby power. **It is possible to design LSTP T-CMOS chip since a key design metric of I_C is exponentially decreased at relatively low N_{ch} region. Moreover, by designing an abrupt channel profile with small ΔR_P, ultra-LSTP and high performance of high and low states can be achieved at the same time owing to fully independent controlled I_{MAX} and I_C.**

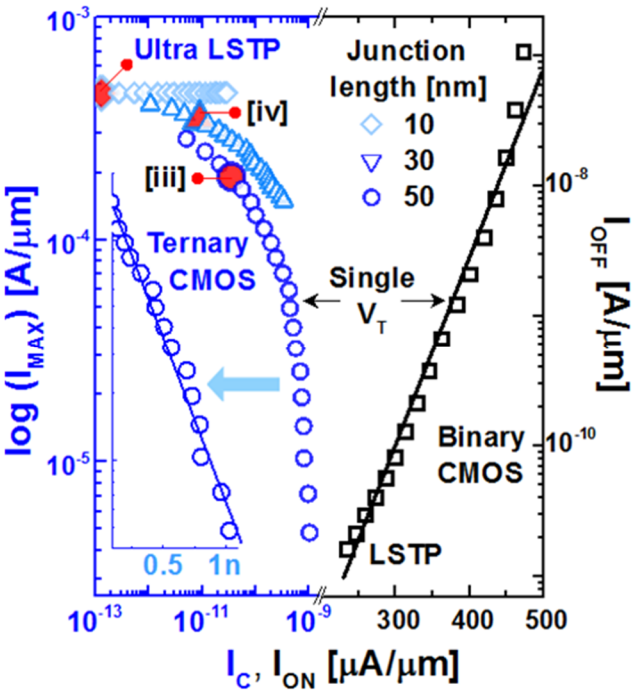


Figure 3.10. T-CMOS design framework based on I_{MAX}-I_C comparing with I_{OFF}-I_{ON} of binary CMOS

3.2 Compact Model of T-CMOS

The measured T-CMOS characteristics in section 3.1 can be reproduced as a clear physical mechanism of BTBT and subthreshold diffusion. Starting with the well-known full analytical models of BTBT and subthreshold diffusion, new compact models of T-CMOS have been developed and verified with experimental data.

3.2.1 Band-to-Band Tunneling Model

The Kane's BTBT model is applied to deal with high doping concentration over 10^{19}cm^{-3} as follow:

$$I_{K,BTBT} = A\frac{\sqrt{2m^*}q^3E_PV_R}{4\pi\hbar^2E_g^{1/2}}exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3qE_P\hbar}\right) = B\cdot E_PV_Rexp\left(-\frac{E_C}{E_P}\right) \tag{3.1}$$

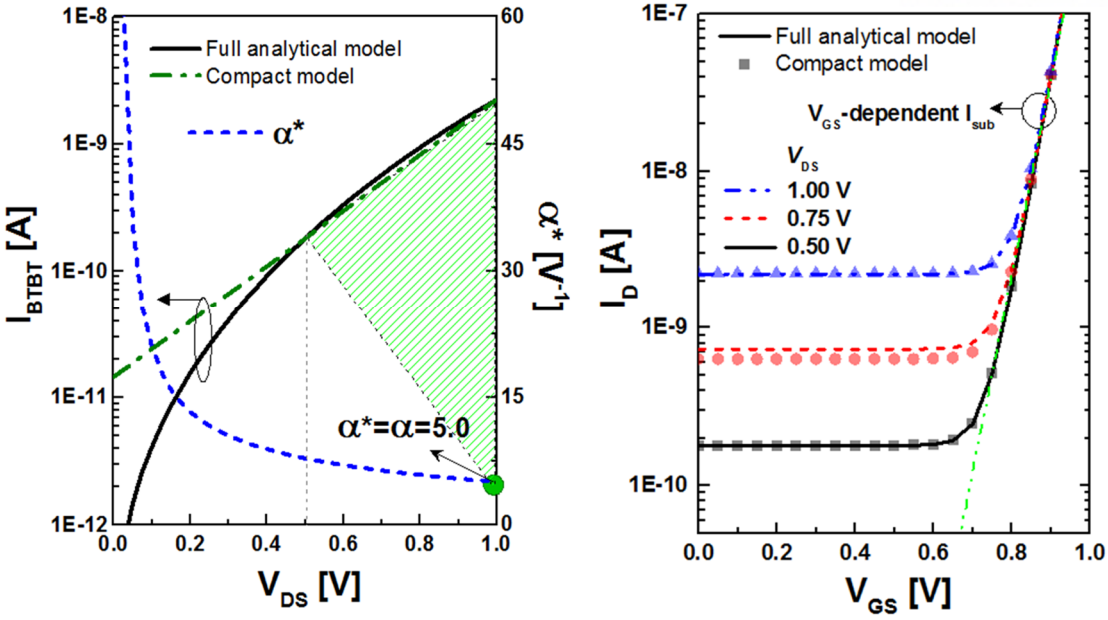
$$E_P = \sqrt{\frac{2qN_{eff}}{\varepsilon_{si}}\left(V_R+\psi_{bi}\right)} \tag{3.2}$$

where A is the area, q is the electrical charge, $m*$ is the reduced effective electron mass, V_R (= V_D) is the reverse biased drain voltage, E_g is the bandgap energy, E_p is the peak field as a function of V_D, N_{eff}= $N_{ch}N_D/(N_{ch}+N_D)$ is effective doping concentration between N_{ch} and drain (N_D), ψ_{bi} is the built-in potential, and ε_{si} is the permittivity of Si. The Eq. (3.1)-(3.2) are assumed the abrupt junction with uniform doping as widely used in the TFET analysis [31].

In the present analytical modeling, the junction parameter (γ) is introduced in the form of γE_p where $0 < \gamma < 1$ for electric field relaxation in the simulated or realistic graded junction. In addition, $\alpha^*(V_{DS})$ and $I_C^*(V_{DS})$ are newly defined by:

$$I_{BTBT}^*\left(V_{DS}\right) = I_C^*exp\left(\alpha^*\frac{V_{DS}}{2}\right) \tag{3.3}$$

$$\begin{aligned}\alpha^*\left(V_{DS}\right) &= \frac{I_{BTBT}\big|_{V_R=V_{DS}} - I_{BTBT}\big|_{V_R=V_{DS}/2}}{V_{DD}/2} \\ &= \frac{2}{V_{DS}}\left[ln\left(2\sqrt{\frac{V_{DS}+\psi_{bi}}{V_{DS}/2+\psi_{bi}}}\right)+\frac{C}{\gamma\sqrt{N_{eff}}}\left(\frac{1}{\sqrt{V_{DS}/2+\psi_{bi}}}-\frac{1}{\sqrt{V_{DS}+\psi_{bi}}}\right)\right]\end{aligned} \tag{3.4}$$



(a) (b)

Figure 3.11. (a) The calculated I_{BTBT}-V_{DS} and (b) I_D-V_{GS} based on full analytical model (Eq. (3.3) and Eq. (3.7)) and compact model (Eq. (3.6) and Eq. (3.8)).

$$I_C^*(V_{DS}) = I_{BTBT}\big|_{V_R = V_{DS}/2} = B\gamma\sqrt{N_{eff}}\sqrt{\frac{V_{DS}}{2}+\psi_{bi}}\left(\frac{V_{DS}}{2}\right)exp\left(-\frac{C}{\gamma\sqrt{N_{eff}}}\frac{1}{\sqrt{V_{DS}/2+\psi_{bi}}}\right) \quad (3.5)$$

Then, for the computational efficiency of the circuit simulation, the compact model for I_{BTBT} can be developed as [32]:

$$I_{BTBT}(V_{DS}) = I_C exp\left[\alpha\left(V_{DS}-\frac{V_{DD}}{2}\right)\right] \quad (3.6)$$

with the constant I_C and α as the compact model parameters. Complementary I_{BTBT} and T-*n*MOS and T-*p*MOS can be described with positive and negative α, respectively. Figure 3.11(a) shows the full analytical I_{BTBT}* with $\alpha^*(V_{DS})$ and I_C* (Eq. (3.3)-(3.5)) and the compact I_{BTBT} model with a constant α and I_C (Eq. (3.6)). **It should be noted that the constant $\alpha = \alpha^*(V_{DS}= V_{DD})$ can produce the well-matched curves at $V_{DD}/2 \le V_{DS} \le V_{DD}$, which guarantee the compact model validity since the only $|V_{DS}| > V_{DD}/2$ range contribute on the voltage transfer in T-CMOS STI circuits.** In the full analytical calculation, the physical device parameters are used as B= 2.2×10^{-13}, C= 7.05×10^{10}, γ= 1 (abrupt junction), N_{eff}= 1.67×10^{19}cm^{-3} (N_{ch}= 2×10^{19}cm^{-3}, and N_D= 1×10^{20}cm^{-3}) and ψ_{bi}= 1.13 V.

3.2.2 Subthreshold Diffusion Model

The compact model for I_{sub} can be developed by following conventional analytical subthreshold current model [33]:

$$I_{sub} * (V_{GS}) = \mu_{eff} C_{OX} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 exp\left[\frac{q(V_{GS}-V_T)}{mkT}\right]\left[1-exp\left(-\frac{qV_{DS}}{nkT}\right)\right] \quad (3.7)$$

where μ_{eff} is the effective mobility, C_{ox} is the oxide capacitance, W/L is the channel width/length, m is the body effect coefficient, K is the Boltzmann's constant, and V_T is threshold voltage. For the analytical device modeling with physical parameters, Eq. (3.7) can have direct relation with I_{EXP} in Eq. (2.1) as

$$\begin{aligned} I_{sub}(V_{GS}) &= \mu_{eff} C_{OX} \frac{W}{L}(m-1)\left(\frac{kT}{q}\right)^2 exp\left[\frac{q(V_{GS}-V_T)}{mkT}\right] \\ &= I_{MAX} exp\left[\beta(V_{GS}-V_{DD})\right] \end{aligned} \quad (3.8)$$

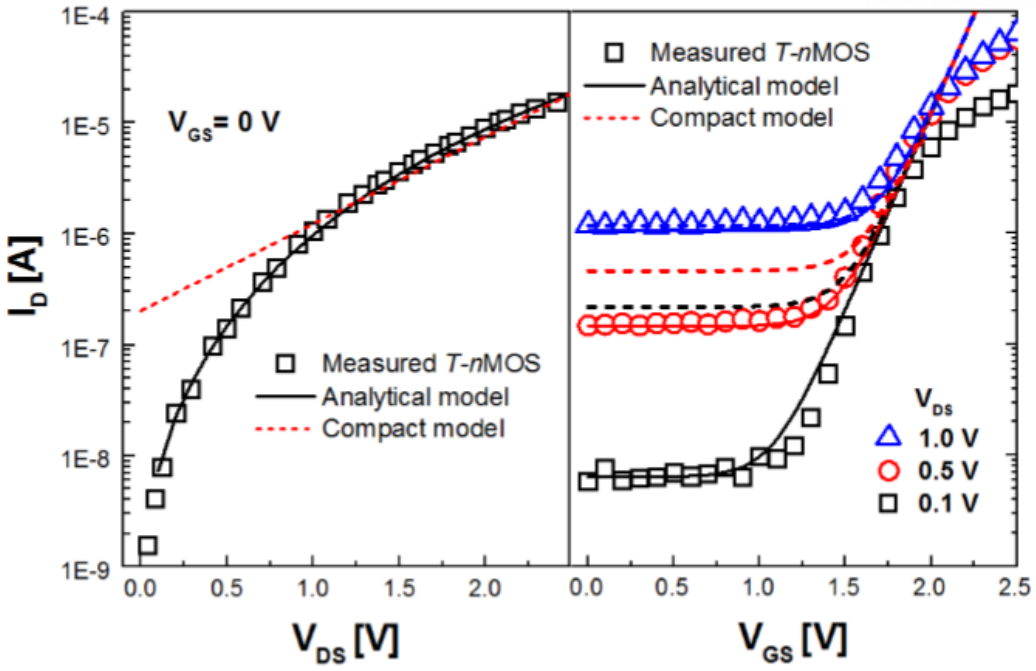
Then, the I_{MAX} can be represented as $I_{MAX}= \mu_{eff}C_{OX}(m\text{-}1)/(kT/q)\exp(\beta(V_{DD}\text{-}|V_T|))$ and β (= q/mkT) corresponds to the SSW. As shown in Fig. 3.11 (b), the V_{DS}-dependent term of $\{1\text{-}\exp(\text{-}qV_{DS}/kT)\}$ can be ignored at $V_{DS} >> kT/q$= 26 mV at room temperature and thus, the V_{DS}-independent compact I_{sub} model is valid.

By using the established compact model, the input voltages in VTC of STI circuits, V_{IL}, V_{IML}, V_{IMH}, and V_{IL} can be derived by complementary combination of T-nMOS and TpMOS current equation: $\{I_{sub} + I_{BTBT}\}_{T\text{-}pMOS} = \{I_{BTBT}\}_{T\text{-}nMOS}$ for V_{IL} and V_{IML}, $\{I_{BTBT}\}_{T\text{-}pMOS} = \{I_{sub} + I_{BTBT}\}_{T\text{-}nMOS}$ for V_{IH} and V_{IMH}. For STI operation conditions of $V_{IL} > 0$ (= GND), $V_{IML} > V_{DD}/2$, $V_{IMH} < V_{DD}/2$, and $V_{IH} < V_{DD}$, the basic criterion for α and β is same with Eq. (2.8) as:

$$\alpha' = \frac{\alpha}{ln(10)} < log\left(\frac{I_{MAX}}{I_C}\right) \Big/ \frac{V_{DD}}{2} << \beta' = \frac{\beta}{ln(10)} \quad (3.9)$$

3.2.3 Verification with Experimental Data

The T-CMOS compact model parameter extraction has been performed as follows: Firstly, from the measured I_D-V_D curves that can be described only by I_{BTBT} (Eq. (3.6)), α = 1.77 can be extracted and



(a) (b)

Figure 3.12. (a) The transfer I_D-V_G and (b) I_D-V_D characteristics of fabricated T-*n*MOS in comparison with full analytical model based on Eq. (3.3) and (3.7) and compact model based on Eq. (3.6) and (3.8).

verified by the calculated value of α^* (V_{DS}= V_{DD}= 2.4 V) in full analytical model as shown in Fig. 3.12(a). Then, β= 11.25 can be directly calculated from the measured SSW from I_D-V_G curves in Fig. 3.12(b). In both, the full analytical model of I_D (V_G, V_D) = I_{sub} (V_{GS}) + I_{BTBT} (V_{DS}) with α^* and β based on Eq. (3.3) and (3.7) well reproduces the measured I_D-V_G and I_D-V_D curves from fabricated T-*n*MOS, since α^* can describe the electric field dependence on whole V_{DS} range. The deviation of the compact model with a constant α = 1.77 at V_{DS} < V_{DD}/2= 1.2 V can be negligible again since the actual operating region of T-CMOS is V_{DS} > V_{DD}/2 during STI operation. The successful STI operation can be expected in that the compact model parameters of T-*n*MOS satisfy the condition of α= 1.77 << β =11.25 (Eq. (3.8)).

3.3 T-CMOS STI

In this section, fabricated T-CMOS-based STI characteristics will be discussed. By using verified T-CMOS compact model in section 3.2, the VTCs of T-CMOS STI are demonstrated and its logic stability is investigated in terms of SNM. In addition, the effect of process-induced OLV on VTCs is studied.

3.3.1 Voltage Transfer Characteristics

Figure 3.13 shows the I_{OUT}-V_{OUT} characteristics at intermediate state transfer ($V_{IMH} < V_{IN} < V_{IML}$) and VTCs according to V_G-dependency of current. The V_{IN}-independent I_{BTBT} of T-*n*/*p*MOS can make only one crossing point on I_{OUT}-V_{OUT} characteristics as shown in Fig. 3.13(a), whereas movement of crossing points are observed in QDGFET with V_{IN}-dependent intermediate current (Fig. 3.13(b)) [24]. In the case

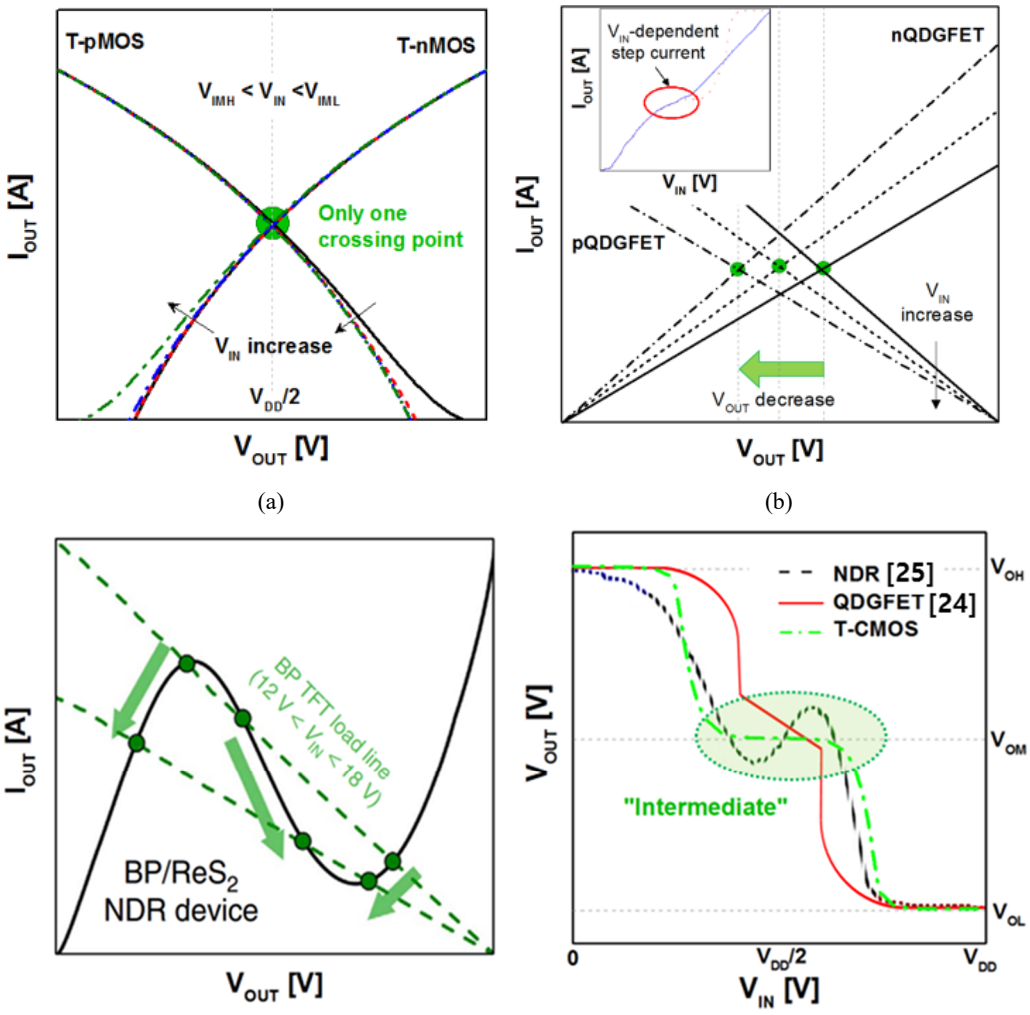


Figure 3.13. The I_{OUT}-V_{OUT} characteristics of (a) T-CMOS inverter, (b) QDGFET-based STI [24], and (c) BF/ReS2 NDR-based STI [25] at intermediate state transfer. (d) The VTCs based on I_{OUT}-V_{OUT} characteristics of (a)-(c).

of BP/ReS_2 NDR devices (Fig. 3.13(c)), three crossing points move different direction, which results in fluctuation of intermediate state [25]. As shown in Fig. 3.13(d), compared with stable intermediate state with voltage gain ($A_V = V_{OUT}/V_{IN}$) = 0 of our T-CMOS STI, the QDGFET and the BP/ReS_2 NDR devices have unstable intermediate states with positive and negative A_V, respectively**.** Therefore, the V_{IN}-independent current is important for stable intermediate state formation in ternary logic.

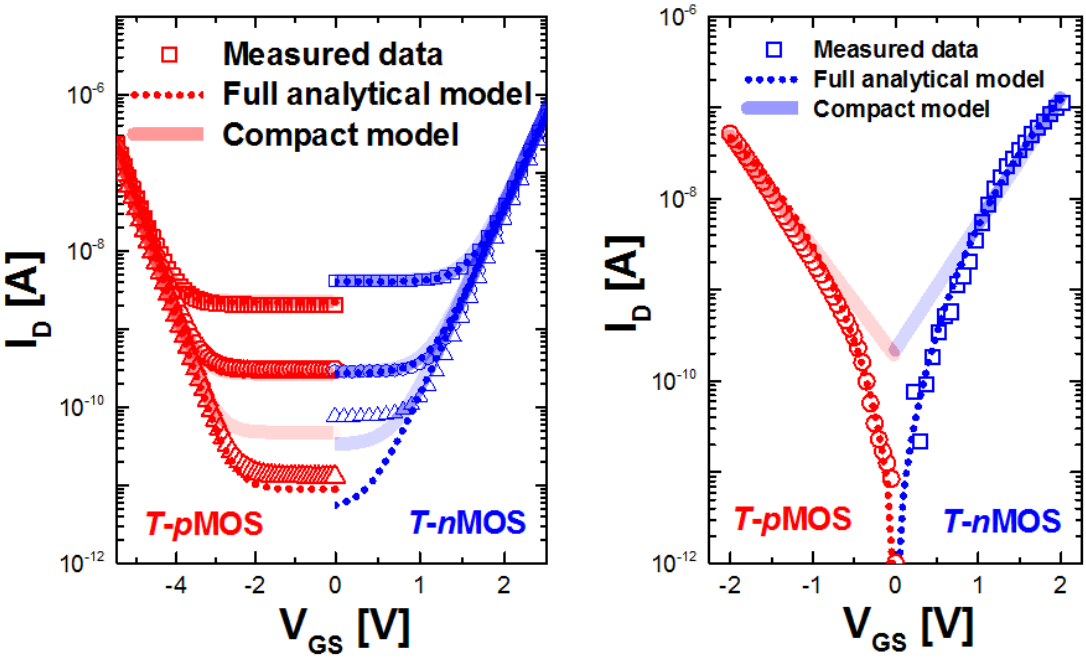
Figure 3.14 demonstrates the VTC of STI based on fabricated T-CMOS of Fig. 3.6(a). As shown in Fig. 3.14(a) and (b), the proposed compact model of Eq. (3.6) and (3.8) well reproduced the complementary T-*n*/*p*MOS. Compared with the VTC based on the full analytical model with α^* (Eq. (3.3)), the compact model with constant α (Eq. (3.6)) can reproduce the completely same characteristics of T-CMOS STI in Fig. 3.14(c). **The identically reproduced I_{BTBT} of fabricated T-*n*MOS of [iii] and T-*p*MOS at $V_{DS} = V_{DD}/2$ by controllable ion-implant process enables stable intermediate state at the exact $V_{OM} = V_{DD}/2$.** Especially, by eliminating the V_G-dependency of the I_{BTBT} completely, the stability of intermediate state is ensured with $A_V = 0$.

The V_{TR}, and V_{IM} of VTC could be derived from T-CMOS compact model of Eq. (3.6) and (3.8), which are identical with Eq. (2.6)-(2.7) as:

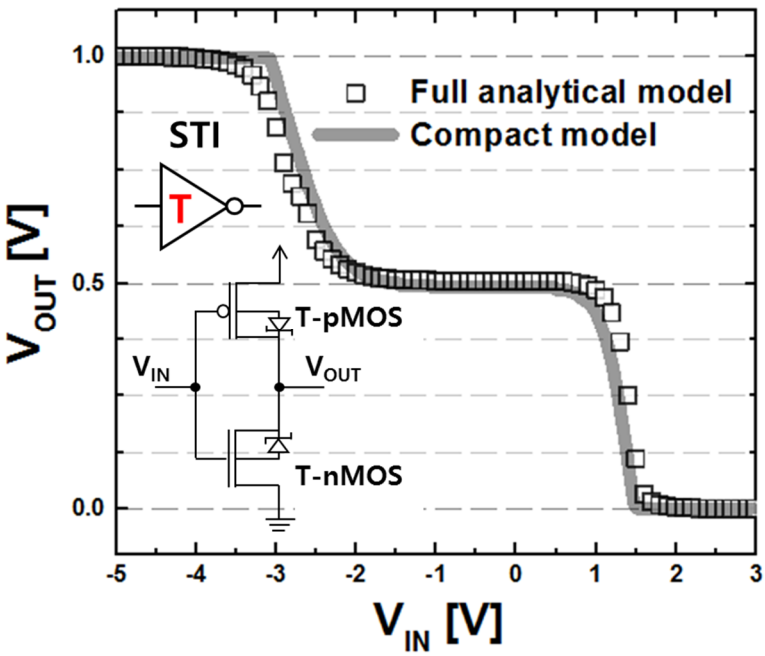
$$V_{TR} = \frac{\alpha}{\beta}\frac{V_{DD}}{2} + \frac{1}{\beta} ln\left(\frac{\beta}{2\alpha}\right) \tag{3.9}$$

$$V_{IM} = V_{DD} - \frac{2}{\beta} ln\left(\frac{I_{MAX}}{I_C}\right) - \frac{2}{\beta} ln\left(\frac{\beta}{2\alpha}\right) \tag{3.10}$$

By enhancing SSW (increase β), the V_{TR} can decrease and subsequently logic states are increase.



(a) (b)



(c)

Figure 3.14. Measured (a) I_D-V_G and (b) I_D-V_D characteristics of fabricated T-*n*/*p*MOS (Fig. 3.6(a)) and in comparison with full analytical model and compact model. (c) Calculated VTCs of T-CMOS STI with full analytical model and compact model

3.3.2 Static Noise Margin

The stability of the logic gate is evaluated in the cross-coupled inverter circuit by SNM [34]-[35], which can be defined as the diagonal of maximum possible square in butterfly curves by mirroring VTCs when worst case noise appeared on all of the logic gates [36]. In ternary logic, four noise margins (NM) of $NM_H/NM_{MH}/NM_{ML}/NM_L$ can be defined at four critical voltages of $V_{IH}/V_{IMH}/V_{IML}/V_{IL}$ where the voltage gain of A_v = -1. Then, the SNM of the proposed STI is determined by the smaller one between NM_H (= NM_L) and NM_{MH} (= NM_{ML}) in symmetric T-CMOS. Since the compact model well described VTC of STI compared with full analytical model in section 3.3.1, the SNM analysis can be done by the compact equation of Eq. (3.6) and (3.8), which can be expressed as

$$NM_H\left(=NM_L\right)=\sqrt{2}V_{IH}=\sqrt{2}\times\frac{1}{\beta'}\left(log\left(\frac{I_{MAX}}{I_C}\right)-\alpha'\frac{V_{DD}}{2}\right) \tag{3.11}$$

$$NM_{MH}\left(=NM_{ML}\right)=\sqrt{2}\times\left(\frac{V_{DD}}{2}-\frac{1}{\beta'}log\left(\frac{I_{MAX}}{I_C}\right)-\frac{2}{\beta'}log\left(\frac{\beta'}{2\alpha'}\right)\right)-\delta \tag{3.12}$$

where δ is the correction factor, as constant, of 30 mV for NM_{MH}. For $NM_H = \sqrt{2}(V_{IH})$, I found that the deviations of the analytical V_{IH} by (3.7) from numerical one including the V_{DS}-dependent term of $\{1-\exp(-qV_{DS}/kT)\}$ in I_{sub} is negligibly small (< 10 mV).

Fig. 3.15 shows the calculated SNM contours in the wide range of α' and β' according to the current ratio between I_{MAX} and I_C at the V_{DD}= 1 V operation. When the current ratio of I_{MAX}/I_C increased, the

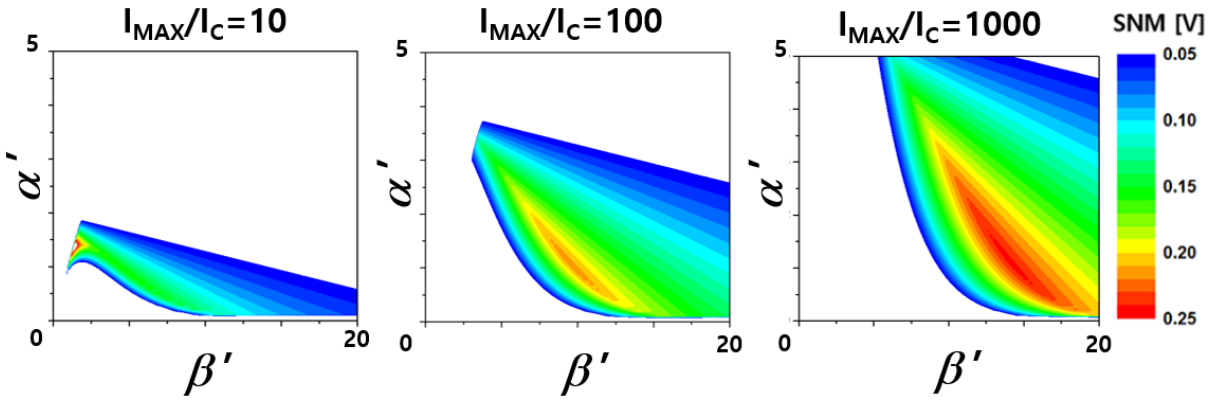


Figure 3.15. The calculated SNM contour in a wide range of a α' and β' with I_{MAX}/I_C of (a) 10, (b) 100, and (c) 1000 at V_{DD}= 1 V based on Eq. (11)-(12).

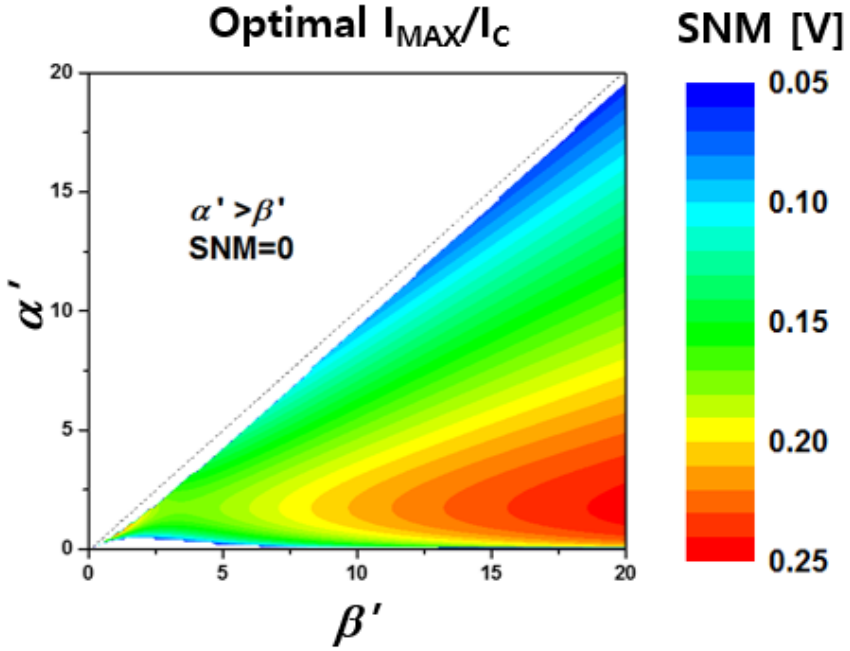


Figure 3.16. The calculated SNM contour in a wide range of a α' and β' with optimal I_{MAX}/I_C at V_{DD}= 1 V based on Eq. (13).

SNM also increase as shown in Fig. 3.15(a)-(c) and the extended design window of α' and β' can be obtained, while SNM decreases below 100mV when the I_{MAX}/I_C < 10. **Thus, it should be noted that V_G-exponentially dependent I_{sub} has the merit to make I_{MAX}/I_C > 10 for stable STI with larger SNM.** In addition, the best SNM condition of $NM_H = NM_{MH}$ results in the optimal I_{MAX}/I_C as function of α' and β' as given by:

$$log\left(\frac{I_{MAX}}{I_C}\right) = (\alpha'+\beta')\frac{V_{DD}}{2} - log\left(\frac{\beta'}{2\alpha'}\right) - 0.01\beta' \tag{3.13}$$

Figure 3.16 shows the best SNM contour according to α' and β' based on Eq. (3.13), where α' << β' can be obtained. The smaller α' and higher β' make the larger SNM.

Figure 3.17 demonstrates the VTC of STI at V_{DD}= 2.4 V based on fabricated T-*n*MOS of [iii] in Fig. 3.6(a) and symmetrically designed T-*p*MOS. The T-*p*MOS is implemented with TCAD device simulator with C_S of 3.65×10^{18} cm^{-3} and C_P of 1.55×10^{19} cm^{-3}. The input range of intermediate sate on VTC is much larger high and low states owing to high V_T, which results in mismatched NM with small NM_H/NM_L of 188 mV and high NM_{MH}/NM_{ML} of 2.88 V, but it can be sufficiently enhanced with T-CMOS design discussed in section 3.1.2

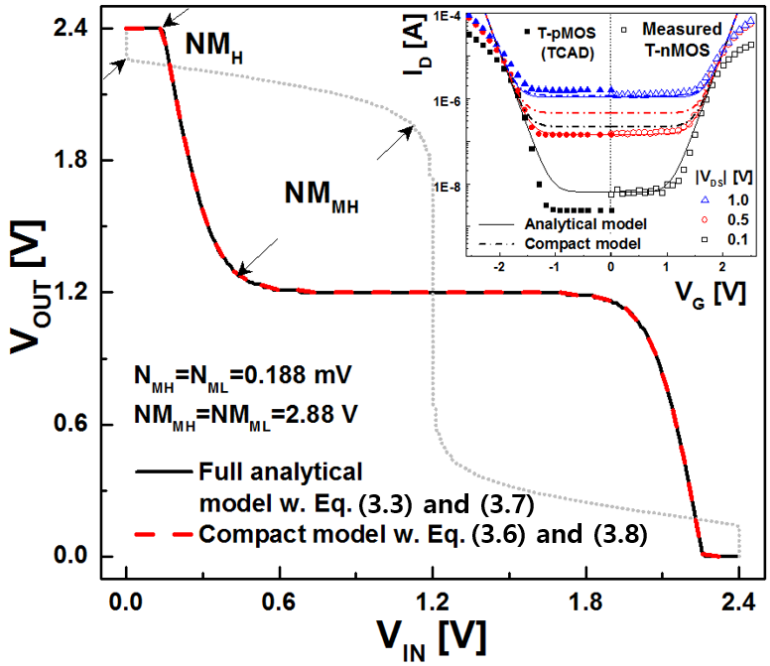


Figure 3.17. The VTCs of STI based on fabricated *T-n*MOS (Fig. 3.6(a)) and symmetrically designed *T-p*MOS.

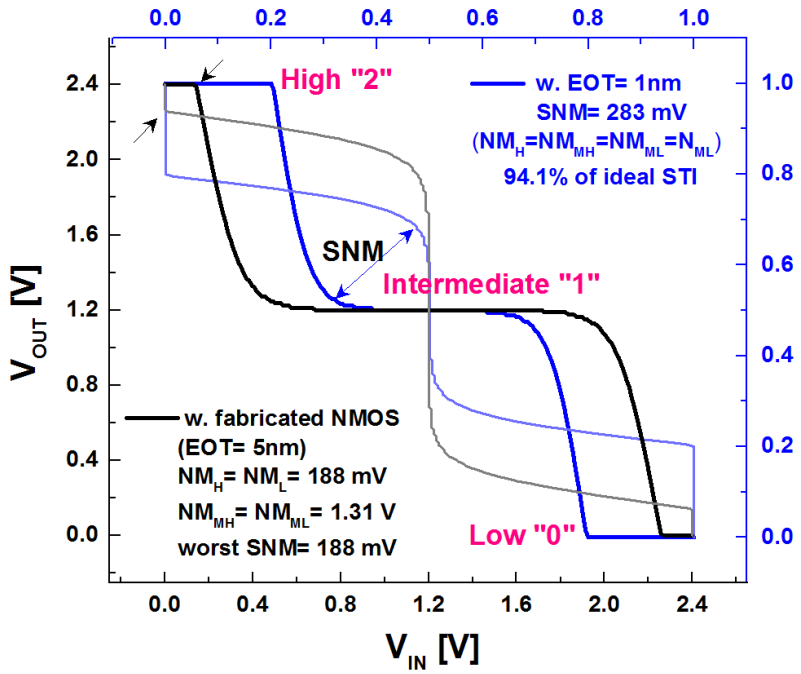


Figure 3.18. The simulated VTC of STI with gate controllability enhanced T-CMOS of Fig. 3.9.

Figure 3.18 shows the simulated VTC of T-CMOS STI based on performance enhanced T-CMOS through the design methodology of Fig. 3.9. It is noted that the β' is dominant factor to determine the SNM and V_{TR} of STI under the sufficiently small α' of 0.77. Only by reducing EOT with 1 nm from Fig. 3.17, SNM increased 282mV (94.1% of ideal STI with SSW= 60mV/dec) with reduced V_{DD} = 1V.

3.3.3 OFF-Leakage Variation from Random Dopant Fluctuation

In the conventional CMOS device technology, it has been recognized that the OLV is hard to be suppressed, since there are complicated OFF-leakage mechanisms and dominant I_{OFF} by I_{sub} (3.7) is exponentially dependent on the inherent V_T variation (σV_T) [37]. In our design of planar CMOS with highly doped N_{ch} for STI operation, however, I have only one clear I_{OFF} mechanism of junction BTBT in a wide bias range [Fig. 3.6(a)]. Based on the analytical of $I_{K,BTBT}$ (Eg. (3.3)), $\Delta I_{K,BTBT}$ as OLV is determined by lower doping variation (ΔN_{ch}) from random dopant fluctuation (RDF), which is the main variability source in planar MOSFETs [38].

Figure 3.19 shows the analytical calculation results of γE_p with γ= 0.573 for graded junction and the corresponding $J_{BTBT} = I_{K,BTBT}/A$ from Eq. (3.3) as a function of N_{eff} including ΔN_{ch} effect. To evaluate ΔN_{ch} for various N_{eff}, I first estimated target dopant (N= $N_{ch}\times L_G\times W\times T_W$) and RDF ($\sigma_N$= ($N_{ch}\times L_G\times W\times T_W$)$^{0.5}$) at 32 nm T-CMOS structure, where T_W is *pn* tunnel junction width. The fluctuated number of dopants as $\Delta N_{ch}/N_{ch}\times 100$ (%) and the resultant OLV of $\Delta J_{BTBT}/J_{BTBT}\times 100$ (%) have been extracted in the inset tables. The universal curves in Fig. 3.19 indicate that even though the number of fluctuated dopants increases according to the increase of N_{eff}, $\Delta N_{ch}/N_{ch}$ decrease from 12.4% to 3.2% in high γE_p regime (> 10^{19} cm^{-3}) and more importantly, OLV is reduced as $\Delta J_{BTBT}/J_{BTBT}\sim$20% while $\Delta J_{BTBT}/J_{BTBT}\sim$92% by $\Delta N_{ch}/N_{ch}\sim$12.4% of RDF in the conventional low N_{ch} =2×10^{18} cm^{-3}.

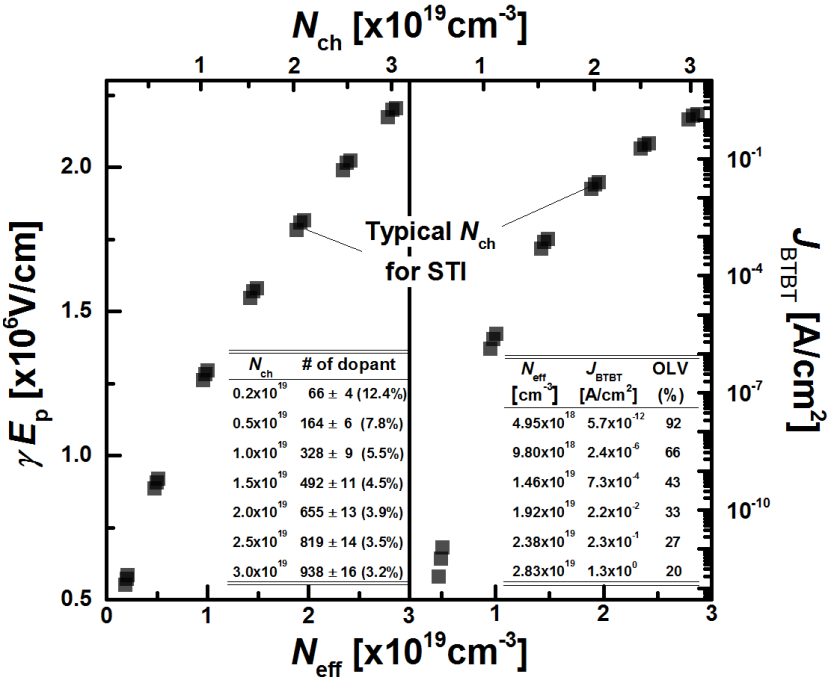


Figure 3.19. Analytical calculation results of γE_p and J_{BTBT} as a function of N_{eff} at V_D = 0.5 V. Inset tables: fluctuated number of dopants as $\Delta N_{ch}/N_{ch}\times 100$ (%) and the resultant OLV of $\Delta J_{BTBT}/J_{BTBT}\times 100$ (%) are summarized.

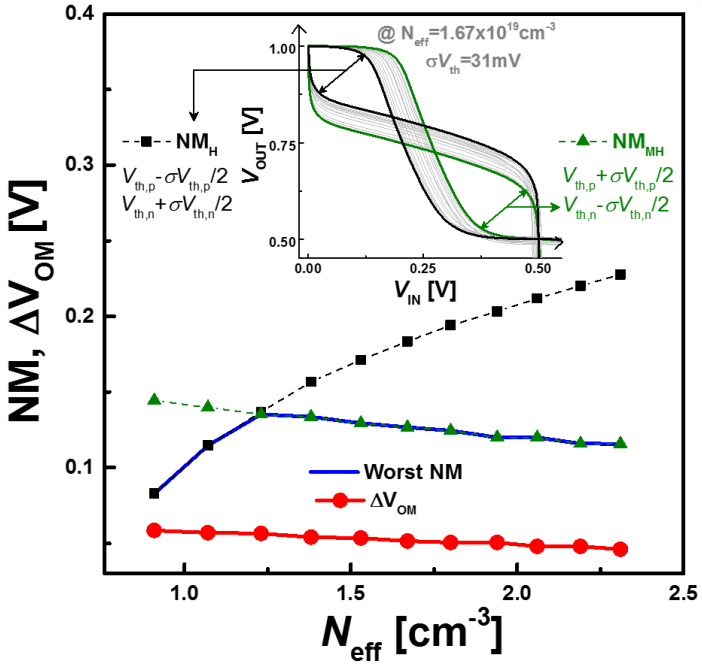


Figure 3.20. Analytical calculation results of ΔV_{OM} and the worst NM between NM_H and NM_{MH} as a function of N_{eff}. Inset: variability example of the calculated VTCs for typical design from σV_T =31 mV in each T-*n*/*p*MOS.

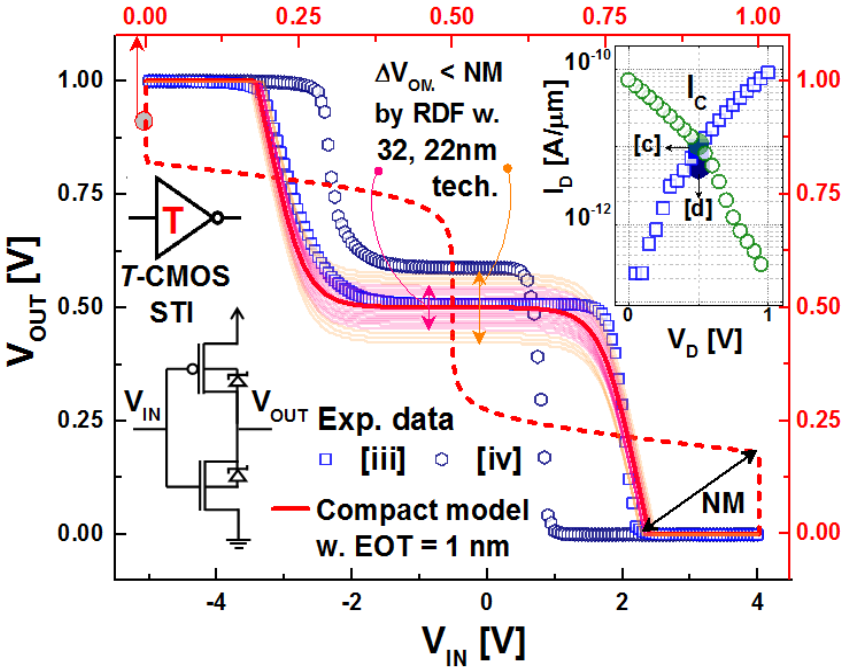


Figure 3.21. VTC of T-CMOS STI considering OLV from process-induced RDF at 32 nm and 22nm technology.

Moreover, **physically oriented logarithmic relation of $V_D^{0.5}$~$1/\ln(J_{BTBT})$ in BTBT mechanism makes V_{OM} variation (ΔV_{OM}) more immune to ΔJ_{BTBT}**. Analytical calculation results of ΔV_{OM}~50 mV when OLV of $\Delta J_{BTBT}/J_{BTBT}$ < 100 % (N_{eff} > 10^{19} cm^{-3}) as shown in Fig. 3.20. It should be noted from Fig. 3.20 that this ΔV_{OM} level of 50 mV from OLV would not be problematic, since it is always below

the worst NM= min(NM_H, NM_{MH}) in the whole feasible N_{eff} range. Here, NM_H and NM_{MH} are independently determined by the respective worst combination of T-*n*/*p*MOS V_T fluctuations from RDF as $\{V_{T,p} - \sigma V_{T,p}/2, V_{T,n} + \sigma V_{T,n}/2\}$ for NMH and $\{V_{T,p} + \sigma V_{T,p}/2, V_{T,n} - \sigma V_{T,n}/2\}$ for NM_{MH}, as shown in the inset of Fig. 3.20.

Figure 3.21 represent VTC of T-CMOS considering OLV from process-induced RDF. Unlike identically designed I_{BTBT} between T-*n*MOS of [iii] and T-*p*MOS of Fig. 3.6(a), T-*n*MOS of [iv] has 1/2 times ΔI_{BTBT} of 1/2 times and results in V_{OM} = 0.6 V. In addition**, stable T-CMOS STI operation is possible at scaled 32 nm and 22 nm technology node with $\Delta V_{OM} < \pm$ 0.1 V.**

3.4 Advanced CMOS technology-based STI

In this section, STI performance investigated with various advanced CMOS structure including bulk/SOI double gate (DG) and tri-gate (TG) FinFET. Figure 3.22(a) and (b) show the bulk and SOI TG ternary FinFET (T-FinFET), respectively [40]. Since the OFF-state constant I_{BTBT} flows from drain to body (Fig. 3.22(c)), it is important to investigate the body effect on the intermediate state in the respective bulk and SOI structure. The floating body of SOI allows the generated carriers from BTBT at drain side (Fig. 3.22(d)) to being recombined once more at source side (Fig. 3.22(e)). Therefore, while bulk FinFET structure with body contact has totally V_G-independent I_{BTBT} at the drain junction (Fig. 3.22(f)), I_{BTBT} of SOI T-FinFET shows a V_G-dependent drain-to-source current component by floating body effect. (Fig. 3.22(g)). From this analysis, it can be concluded that the mainstream low-cost bulk FinFET technology can be more suitably adopted as T-CMOS technology platform for the stable STI operation with completely V_G-independent I_{BTBT}.

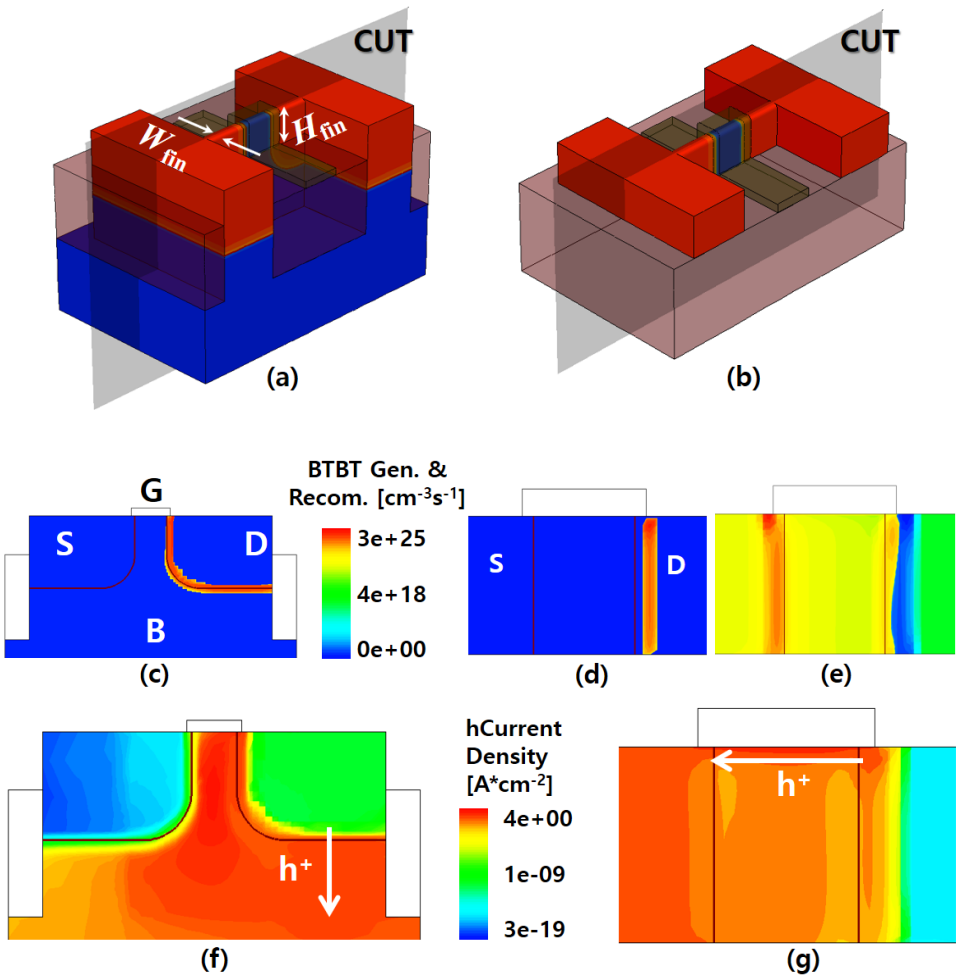
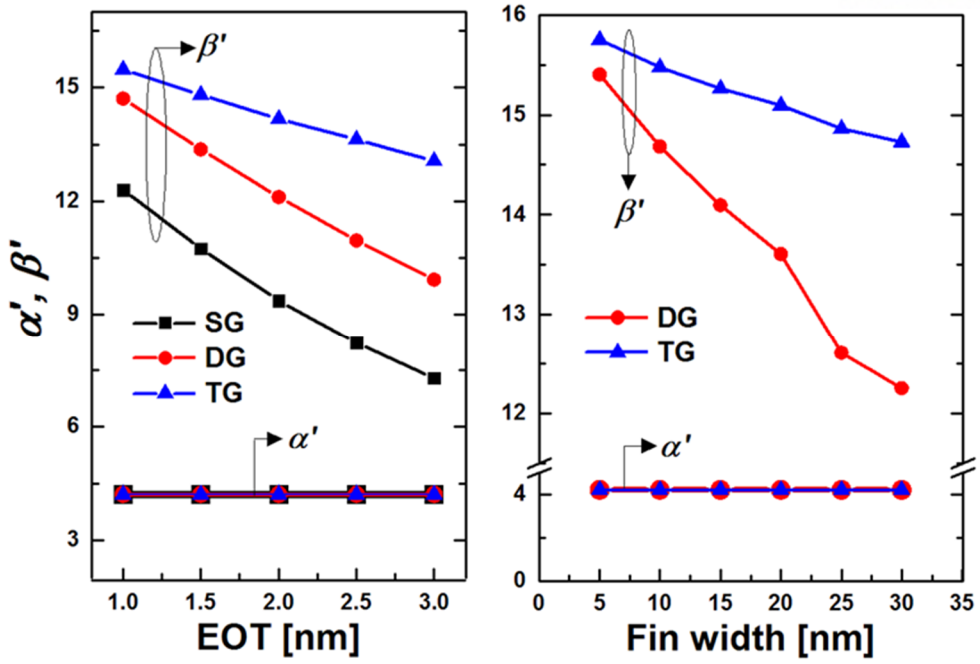


Figure 3.22. (a) 3D structure of bulk and (b) SOI *T*-FinFET (c) BTBT gerneration and recombination rate in bulk and (d)(e) SOI *T*-FinFET (f) hole current density of bulk and (g) and SOI *T*-FinFET.



(a) (b)

Figure 3.23. Device design of α' and β' according to physical parameters of (a) EOT and (b) Fin width (Si thickness) at SG, DG, and TG CMOS structures.

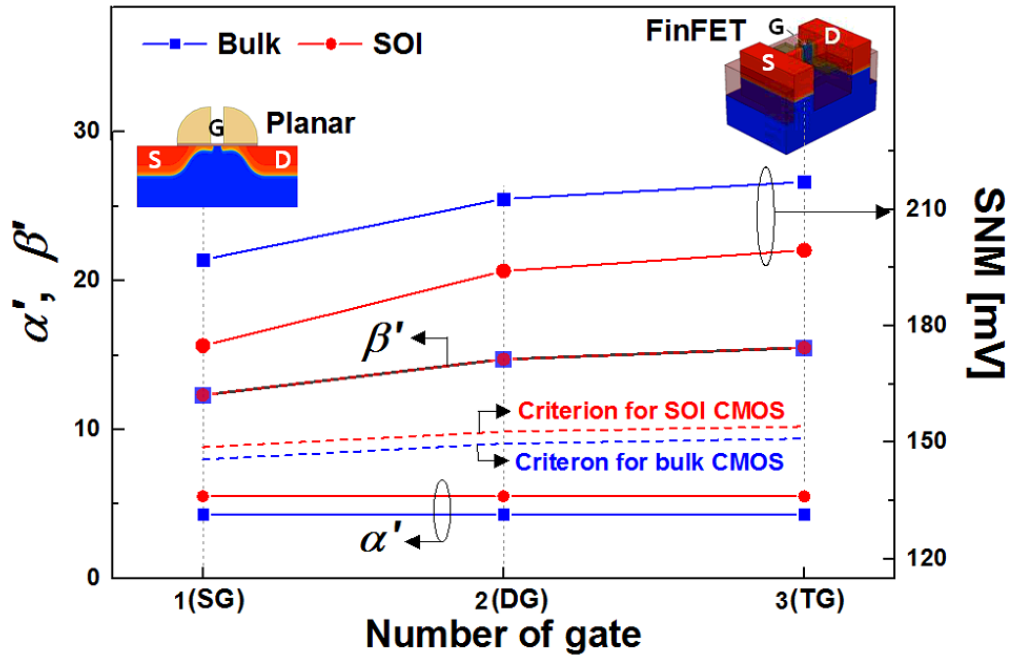


Figure 3.24. The SNM enhancement of bulk/SOI SG T-CMOS and DG/TG *T*-FinFET structure with the EOT= 1 nm.

For higher β' (lower SSW), EOT and fin width (W_{fin}) should be scaled down as shown in Fig. 3.23. The device simulation was performed by Synopsys Sentaurus with nonlocal BTBT modeling including bandgap narrowing based on design parameters of L_G= 32 nm, EOT= 1 nm, W_{fin}= 10 nm, H_{fin}= 60 nm,

and uniform channel profile (N_{ch}) = 2×10^{-19} cm^{-3}. At here α' (= 4) are relatively overestimated than measured T-CMOS (α' = 0.77). The β' can be improved from 5.6 to 15.3 by scaling the EOT to 1 nm in single-gate (SG) *T*-CMOS (Fig. 3.23(a)), and TG *T*-FinFET further increased β' up to 15.57 at W_{fin}= 5 nm (Fig. 3.23(b)). Figure 3.24 shows the SNM enhancement in advanced *T*-CMOS STI based on Eq. (2). In the SOI structures, SG *T*-CMOS STI and DG/TG *T*-FinFET STIs have SNMs of 76 %, 84.4 %, and 86.7% of ideal SNM (=230 mV with β'= 16.7 (SSW= 60 mV/dec)) owing to relatively high α' of 5.5 at V_{DD}= 1 V, whereas the SNMs of bulk *T*-CMOS STI and *T*-FinFET STI increased as 85.6 %, 92.5%, and 94.4% respectively, owing to completely V_G-independent I_{BTBT} and small α'.

3.5 Supply Voltage Scaling for Ultra-Low Power Application

In principle, the driving currents of our STI circuit based on the OFF-state current mechanism (I_{BTBT} and I_{sub}), which should be enhanced for higher speed, can be designed for optimization between delay and power in the subthreshold OFF-current level. By focusing on the low-power consumption, the proposed STI is targeted for LSTP application with a resolved P_S (= $I_{K,BTBT} \times V_{DD}$) by designing $I_{K,BTBT}$ ($V_D = V_{DD}$) ~ 50 pA of LSTP requirement in ITRS [27]. In the viewpoint of standby power per bit (P_S/bit), the proposed STI shows 2/3 times reduced P_S than that of binary logic gates, since it has the identical number of gates (two) and supply V_{DD} (one) as in the conventional binary CMOS inverter. Meanwhile, our STI with a half voltage swing (V_{DD}/2) can have 1/4 times reduced P_D for each logic transition under a single V_{DD} since $P_D \sim C_L V_{DD}^2$. Thus, for ultimate low-power application, it is important to investigate the minimum V_{DD} ($V_{DD,min}$), which is achievable in our STI. As shown in Fig. 3.25, the loading capacitance (C_L) can be assumed as 1 fF level in the 32 nm CMOS, which is the reduced value from the maximum capacitance ($C_{max} = C_{ox}$) in our STI operation voltage (0~1 V) even though the minimum capacitance (C_{min}) is increased by the reduction of the depletion width as N_{ch} increases. In case of binary CMOS inverter, it is well known that V_{DD} scaling is limited by thermal noise as $V_{DD,min} > (2\text{-}4)kT/q$, which means $V_{DD,min} > 50\text{-}100$ mV at T = 300 K, since both transistors operate in subthreshold regime with a thermal diffusion during voltage transition [41]. In the proposed STI, however, different current mechanisms of junction BTBT leads to distinct $V_{DD,min}$ by 1/Av =-1 at $V_{OUT} = V_{DD}/4$ from $I_{K,BTBT,n} + I_{sub,n}$

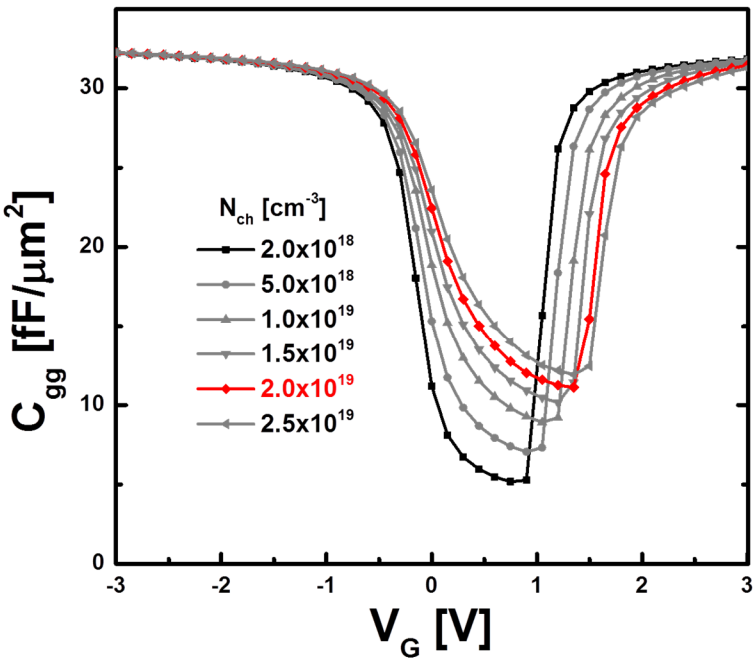


Figure 3.25. Simulation results of C_{gg}-V_G characteristics as N_{ch} increases.

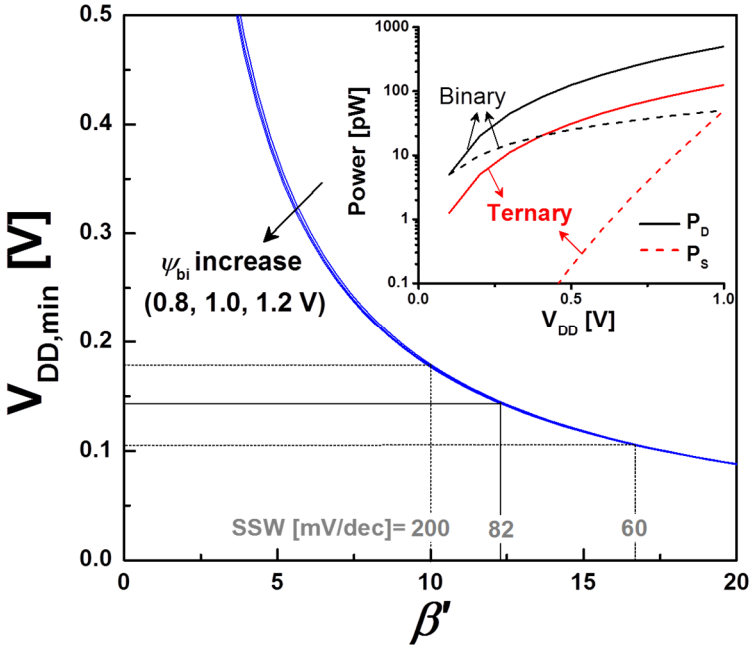
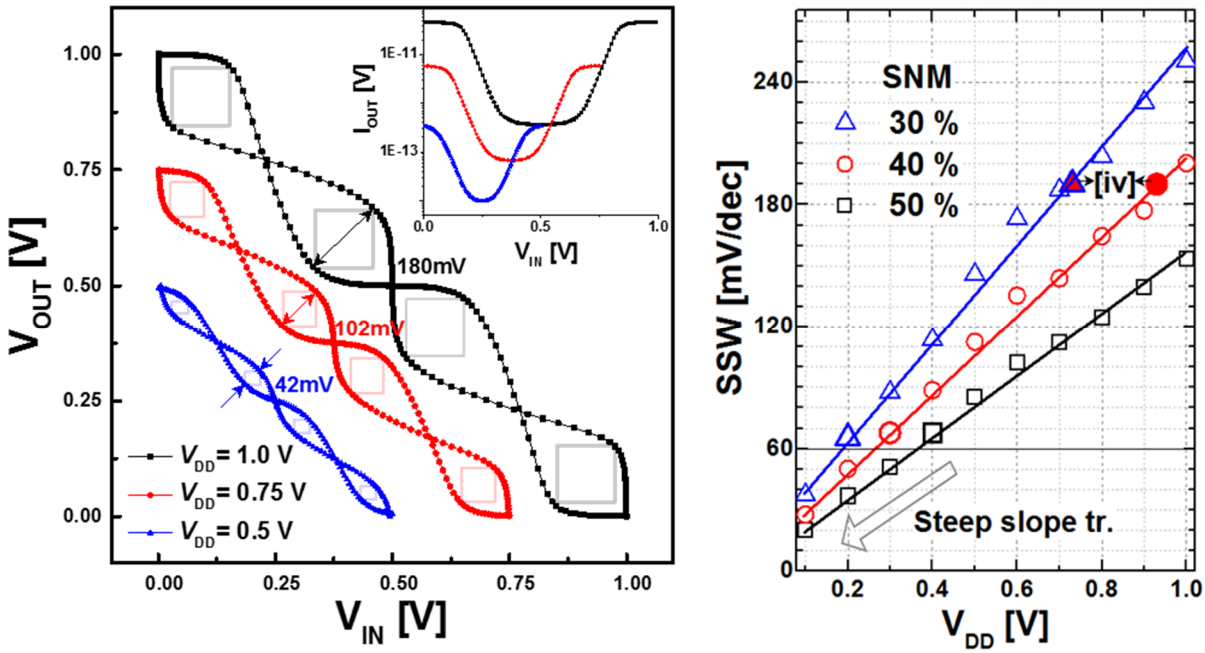


Figure 3.26. Calculation results of $V_{DD,min}$ as a function of β' with ψ_{bi} =0.8, 1, and 1.2 V, respectively. Inset: expected low-power consumption of P_S and P_D as V_{DD} scaling down in comparison with the ternary and binary inverter.

= $I_{K,BTBT,p}$. During the derivation of $V_{DD,min}$ from this condition with Eq. (3.3) and (3.7), it becomes $V_{DD,min}$ (β', ψ_{bi}) as a function of β'-related SSW and α'-related ψ_{bi}. Fig. 3.26 shows the calculation results of $V_{DD,min}$ in the feasible β' range, which indicate that $V_{DD,min}$ can be reduced for lower SSW and less dependent on ψ_{bi}. This is reasonable in that the condition of 1/Av= dV_{IN}/dV_{OUT}= -1 is applied at V_{OUT} = V_{DD}/4 in the transition region where SSW or β' effect is dominant as shown in V_{TR} of Fig. 2.5(a). The achievable $V_{DD,min}$ of STI is saturated around 100 mV, which is similar with the conventional CMOS inverter. As shown in Fig. 26 (inset), however, P_S of our STI can be dramatically reduced down to 1/100 times when considering measurable OFF-current level, since junction BTBT-based I_{OFF} exponentially decreases according to V_{DD} reduction, while the subthreshold I_{OFF} in the conventional CMOS is not dependent on V_{DD}.

Figure 3.27(a) shows the calculated VTC of V_{DD} scaled T-CMOS based on Eq. (3.3) and (3.7). Theoretically, T-CMOS STI can be scaled down to V_{DD}~ 0.1 V, however SNM also decreased. To obtain sufficient SNM for logic stability, the SSW of T-CMOS should be improved as shown in Fig. 3.27(b). At V_{DD}= 0.3 V operation, T-CMOS STI with SSW= 70mV/dec has 40 % SNM of ideal SNM (= √2xV_{DD}/4). By applying the OFF-state I_{BTBT} on steep slope transistors, continuous power scaling is possible with sufficient SNM.

Figure 3.28 compares the P_S of *T*-CMOS STI with CNTFET [21], and QDGFET [22],[24]. The CNTFET and QDGFET-based STI has high P_S at intermediate "1"-states rather than high "2" and low



(a) (b)

Figure 3.27. (a) Calculated VTCs of V_{DD} scaled T-CMOS with SSW= 80 mV/dec and (b) SSW enhancement for V_{DD} scaling of T-CMOS with sufficient SNM (30, 40, 50% of ideal STI).

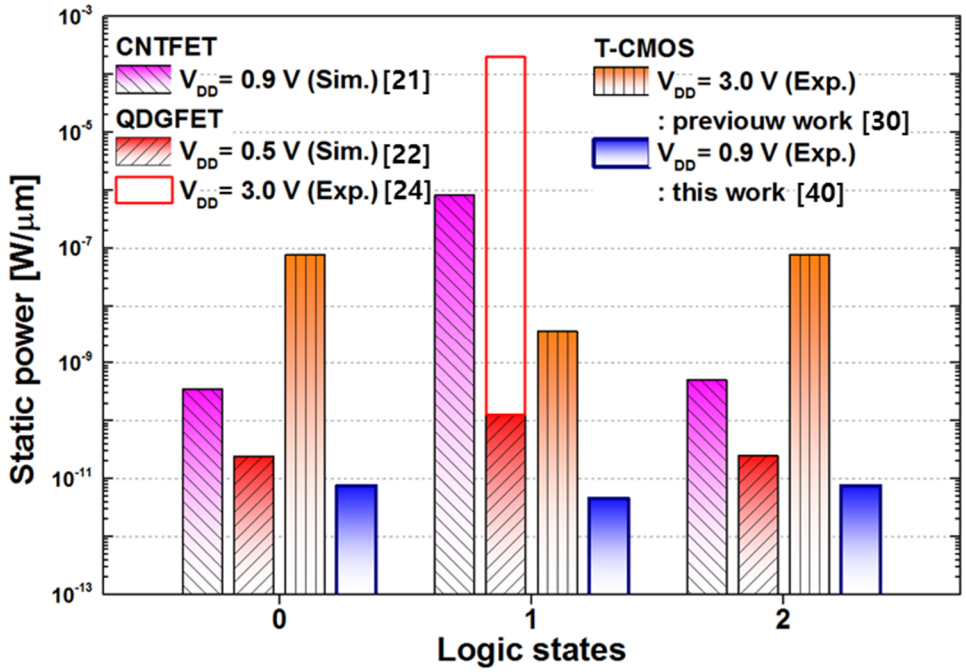


Figure 3.28. Comparison results of STI static power consumption with CNTFET [21], QDGFET [22], [24], and *T*-CMOS at V_{DD}= 3.0 and 0.9 V at each logic states ("0", "1", and "2").

"0" states, since both have voltage dividing at ON-state constant current. Especially, the experimental results of QDGFET increase P_S over 100 μW/μm [24], thus additional transistor for static current cut-off was required to decrease P_S down to 100 pW/μm [22]. On the other hand, the P_S of *T*-CMOS STI

increased at "0" and "2" states rather than "1"-state owing to electric field-dependent I_{BTBT}. However, the remarkably low pA/μm-level I_{BTBT} makes *T*-CMOS STI suitable for ultra-LSTP applications with P_S= 7.7 pW/μm (average P_S= 6.6 *p*W/μm) by 1/10^6 times reduction in comparison with P_S ~ 1 μW/μm from CNTFET-based STI. Even compared with T-CMOS STI at V_{DD}= 3V, this pW-level P_S is 1/10^4 times reduced by OFF-state I_{BTBT} and V_{DD} scaling (V_{DD}= 0.9V).

The quantitative comparison results of the proposed STI with the previous STI works as introduced in Section I have been summarized in Table 3.1. In terms of the compactness, our STI has the smallest number of components as in binary CMOS inverter with only N = 2 elements under single V_{DD}, which can be scaled down to 0.1 V by the proposed principle. Therefore, the lowest power consumption can be achieved as P_S~ 1 fW and P_D~ 5 pW at the scaled V_{DD}= 0.2 V in the proposed STI.

Table 3.1. Comparison of the compactness and low-power consumption capability of the proposed STI

Group	Device type	*N*: # Tr.	# of V_{DD}	V_{DD} [V]	I_{OFF} [A]	P_S= NI_{OFF} V_{DD} [W]	α^*	C_L [*f*F]	P_D= $f\alpha C_L$ x(V_{DD}/2)^2[W]
This work	CMOS	2	1	1	5.00×10^{-11}	5.00×10^{-11}	1	1	1.25×10^{-10}
				0.5	3.68×10^{-13}	1.84×10^{-13}			3.13×10^{-11}
				0.2	5.87×10^{-15}	1.17×10^{-15}			5.00×10^{-12}
[15]	CMOS	3	2	2	2.00×10^{-5}	4.00×10^{-5}	1.5	1	7.50×10^{-10}
[16]	DECMOS	4	2	2	4.51×10^{-12}	9.02×10^{-12}	2	1	1.00×10^{-9}
[17]	CMOS	4	2	8	3.33×10^{-4}	2.67×10^{-3}	2	1	1.60×10^{-8}
[18]	CNTFET	4	1	1.5	7.50×10^{-6}	1.13×10^{-5}	2	0.01**	5.63×10^{-12}
								1	5.63×10^{-10}
[19]	SET	4	3	8	2.00×10^{-8}	1.60×10^{-7}	2	0.01**	1.60×10^{-10}
								1	1.60×10^{-8}
[21]	CNTFET	6	1	0.9	9.21×10^{-7}	8.29×10^{-7}	3	0.01**	3.04×10^{-12}
								1	3.04×10^{-10}
[22]	QDGFET	3	1	0.5	2.56×10^{-10}	1.28×10^{-10}	1.5	1	4.69×10^{-11}
		2			2.00×10^{-4}	1.00×10^{-4}			

*α is the activity factor, which is assumed to be proportional to *N* (:# of elements) in each STI circuit for P_D with same *f*= 500 kHz.

** C_L of CNTFET and SET has been assumed to be 0.01 times lower than that of CMOS owing to their relatively small dimension.

Chapter 4. T-CMOS Application

4.1 Multi-Valued Logic Circuits

The proposed STI can replace the binary circuit applications with revolutionary decreased number of device and circuit interconnection. As an example, I investigate ternary logic gates and 3-bit analog-digital converter circuits.

4.1.1 Ternary Logic Gate

The general ternary logic gate of STI, minimum (MIN), and maximum (MAX) have same functions of inverter, AND, and OR gates in binary logic. Thus, STI, not MIN (NMIN) and not MAX (NMAX) gates are easily implemented from inverter, NAND, and NOR gate by substituting the binary CMOS with proposed *T*-CMOS. Figure 4.1 shows the NMIN and NMAX circuit schematics and symbols. In general, intermediate state caused by voltage dividing varies depending on circuit configuration owing to voltage drop at floating nodes of V_X and V_Y in Fig. 4.1, thus ternary device design should be changed according to all application circuits or required compensating circuits. But, T-CMOS logic gates with common-body scheme can transfer stable intermediate state. Figure 4.2 compares the effects of the common-body and body-source contact of T-CMOS MIN and MAX. As shown in transient simulation, common-body scheme can ignore voltage drop in floating node.

Table 4.1 and 4.2 summaries the delay and power analysis of high performance (HP) and low power (LP) ternary logic gate, respectively. For the HP ternary logic design, the model parameters of α'= 2, β'= 14.2, I_C=100 *n*A, and I_{MAX}= 30 μA are used based on HSPICE BSIM4 model (level 54) [42], while LSTP ternary logic gate was designed with I_C= 1 *n*A, and I_{MAX}= 1 μA. For the timing analysis, transient

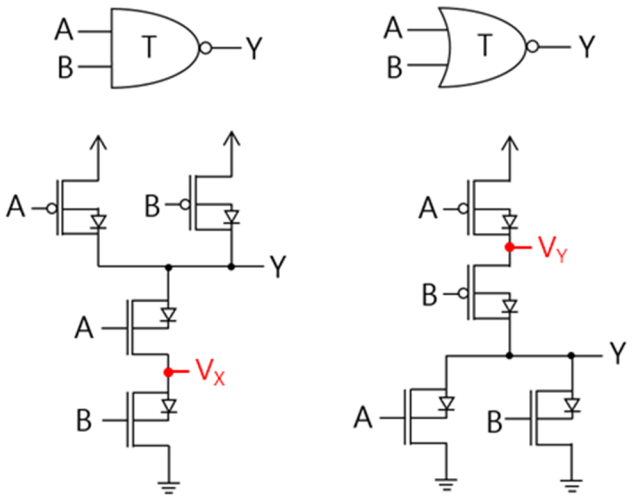


Figure 4.1. The circuit symbols and schematics of (a) NMIN and (b) NMAX

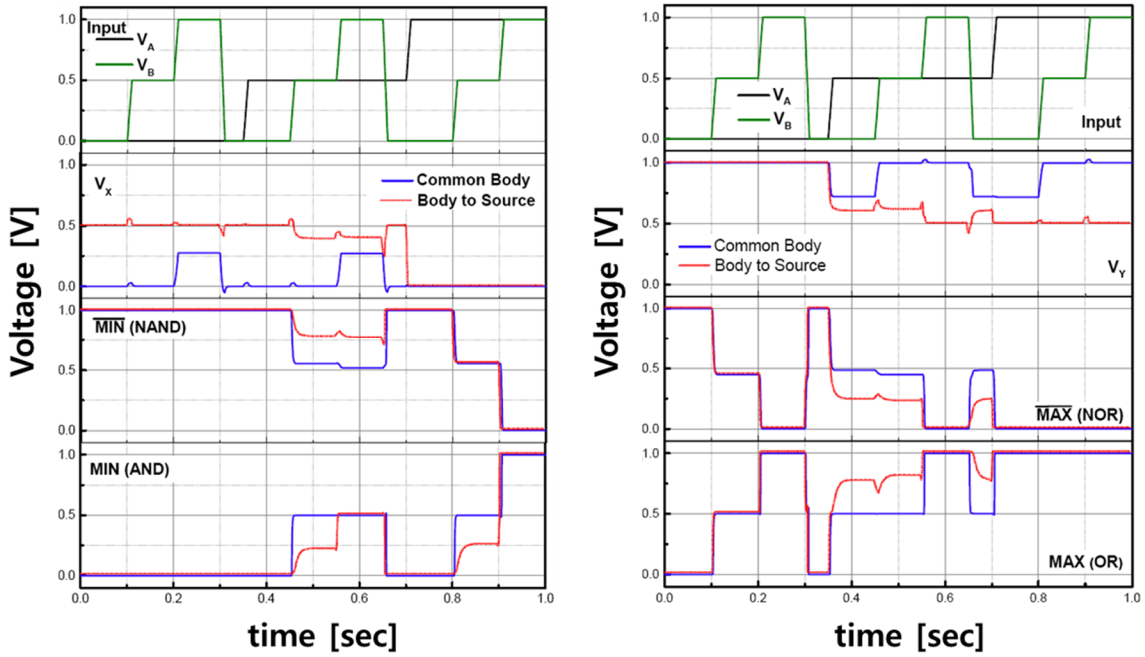


Figure 4.2. Transient simulation results of T-CMOS (a) MIN and (b) MAX gates compared the effect of common-body and body-to-source contacts.

Table 4.1. High performance ternary logic gate

Logic gate	STI		NMIN		NMAX	
	τ_0[ps]	χ[ps/fF]	τ_0[ps]	χ[ps/fF]	τ_0[ps]	χ[ps/fF]
0→1	67.1	2.63	94.2	0.89	100	2.74
1→2	5.7	0.03	8.7	0.03	17.5	0.10
2→1	69.5	2.41	105.6	1.86	102	1.03
1→0	2.7	0.02	9.25	0.05	4.2	0.01
0→2	9.42	0.14	13.8	0.11	25.5	0.30
2→0	5.0	0.06	13.9	0.13	6.3	0.05

simulation of six-input transition (0→1, 1→2, 2→1, 1→0, 0→2, and 2→0) have been performed with rising/falling time (t_r/t_f) of 1*p*s. The intrinsic delay (τ_0) and linear coefficient (χ) are extracted based on 50%-50% propagation delay method for the linear delay model according to the load capacitance (C_L):

$$\begin{aligned} \tau_d &= \tau_0 + \chi C_L \\ C_L &= C_{OUT} + \sum_i C_{in,i} \qquad where\ \ i \in fanout \end{aligned} \tag{3.13}$$

The worst delays are observed in 0→1and 2→1transitions owing to relatively lower I_{BTBT}.

In Table 4.2, the input (C_{in}) and ouput capacitances (C_{out}) are extracted from C-V simulation by using *T*-CMOS compact model, which are confirmed by the calculated C_{gg} = 0.345 *f*F and drain capacitance ($C_{dd} \sim C_{gg}/3$) from the EOT of 1 *n*m. The P_S is estimated with average value of three output sates ("0", "1", and "2") in ternary logic gate. The P_D are calculated with switching activity of 0.1 and operating frequency (*f*) of 10MHz.

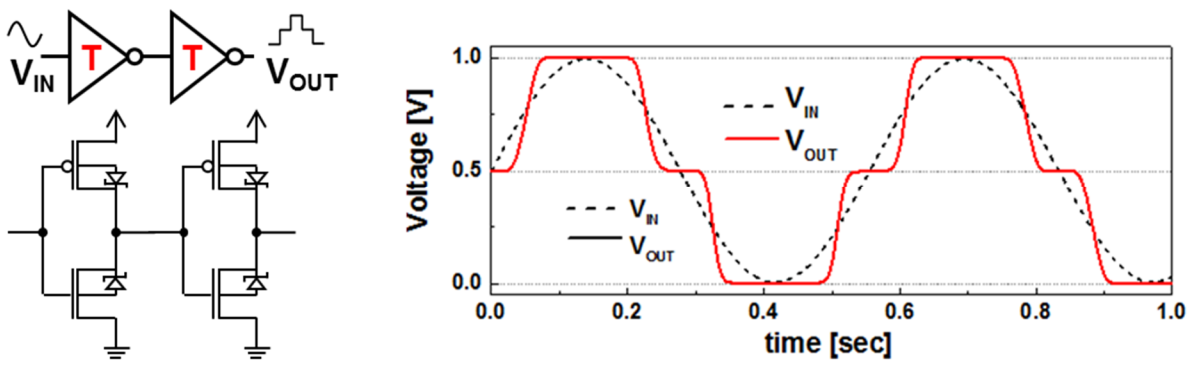
Table 4.2. Low power ternary logic gate

Logic gate	STI	NMIN	NMAX
C_{in} [*f*F]	0.7	0.7	0.7
C_{out} [*f*F]	0.24	0.36	0.36
P_S [*n*W]	7	14	14
P_D [*n*W]	0.24	0.27	0.27

P_D is calculated with f= 10MHz, and switching activity of 0.1

4.1.2 Novel Analog-To-Digital Converter Circuits

As an example of revolutionary decreased number of device and circuits, I demonstrate 3-bit analog-to-digital converter (ADC) circuit is demonstrated based on T-CMOS STI. Binary logic conventionally required 2 comparators with 20 transistors for quantizer circuits and additional 2 XOR and 2 OR gates for encoder circuit [43] however, this work required only two STIs with four T-*n*/*p*MOS as shown in Fig. 4.3. The proposed 3-bit ADC circuits has only 9.6% area of binary 3-bit ADC. For the power-delay-product (PDP) enhanced ADC circuit, additional binary *n*/*p*MOS (M_{N1} and M_{P1}) are introduce in Fig. 4.4. As shown in Fig. 4.4 (inset), the M_{N1} suppressed static current untill MOSFET OFF-current level



(a) (b)

Figure 4.3. (a) T-CMOS based 3-bit ADC circuit and (b) its transient simulation results.

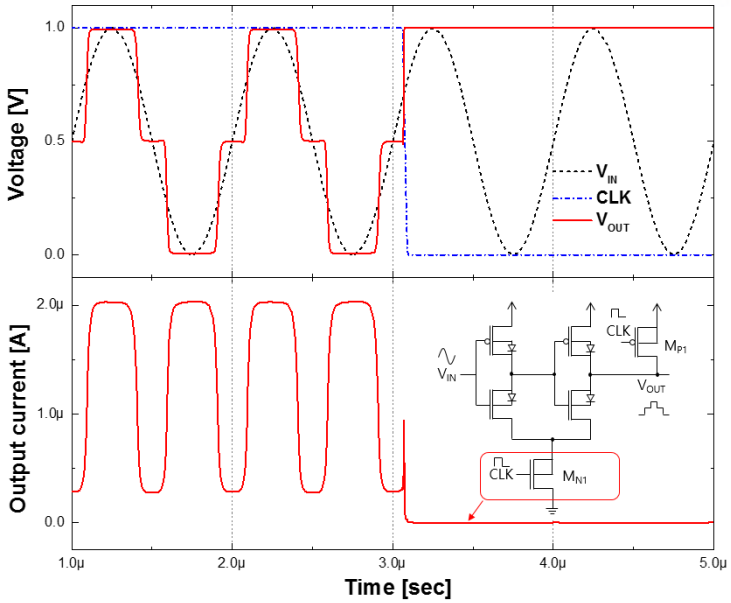


Figure 4.4. Transient simulation results of compact 3-bit ADC with static current path of M_{N1}.

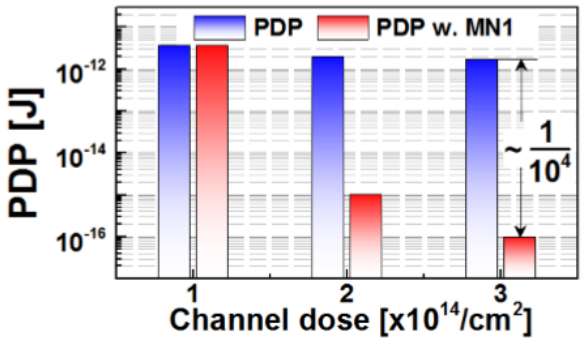


Figure 4.5. PDP analysis of ADC circuits. M_{N1} enhance the PDP up to 10^{-4} at channel dose of 3×10^{14}cm^{-2}.

Table 4.3. Performance analysis of ADC according to channel conditions.

Dose[cm^{-2}]	I_C [A]	τ [s]	I_{static} [A]	P_S [W]	PDP [J]
$1x10^{14}$	9.1×10^{-11}	1×10^{-2}	1×10^{-9}	1×10^{-9}	1×10^{-11}
$2x10^{14}$	1.4×10^{-7}	1×10^{-6}	1×10^{-9}	1×10^{-9}	1×10^{-15}
$3x10^{14}$	1.3×10^{-6}	1×10^{-7}	1×10^{-9}	1×10^{-9}	1×10^{-16}

(I_{OFF}~1 nA) during the OFF-clock signal. Table 4.3 represents performance analysis of ADC according to channel implant conditions. Since the worst τ of ADC is determined by I_C (I_{BTBT} @V_D= V_{DD}) and P_S is determined by I_{OFF} of M_{N1}, the PDP can be further reduced with high channel dose and abrupt junction. By blocking the static current path with clock-synchronous M_{N1}, PDP of ADC has been extremely enhanced from 10^{-12} to $1x10^{-16}$ J (Fig. 4.5).

4.2 Five Memory State Using Double Peak Negative Differential Resistance (NDR) Devices and T-CMOS STI

I propose complement double-peak negative differential resistance (NDR) devices with ultra-high peak-to-valley current ratio (PVCR) over 10^6 by combining tunnel diode with conventional CMOS and its compact 5-state latch circuit by introducing T-CMOS STI. At the "high"-state of STI, *n*-type NDR device (tunnel diode with *n*MOS) has first NDR characteristics with first peak and valley by BTBT and trap-assisted tunneling (TAT), whereas *p*-type NDR device (tunnel diode with *p*MOS) has second NDR characteristics from the suppression of diode current by OFF-state MOSFET. The "intermediate"-state of STI permits double-peak NDR device to operate 5-state latch with only 4 transistors, which has 33% area reduction compared with that of binary inverter and 57% bit-density reduction compared with binary latch.

4.2.1. Challenges of NDR Devices

The NDR devices are promising alternative device performing multifunctional operation based on its nonmonotonic behavior [44]-[48]. Since the tunnel diode with NDR characteristics has been discovered by Esaki [49], there have been in problems for practical applications owing to low PVCR below 10 by TAT current through forbidden band-gap and CMOS incompatible process or compound materials [50]-[52]. For the improvement of PVCR over 100 based on CMOS compatible process, many research works have been reported focusing on the MOSFET structures. Enhanced surface generation in SiGe-based gate diode is exploited for PVCR of 300 around at 3V [53], and the breakdown mechanism of gated bipolar device shows PVCR of 10^3 at 2.5V [54]. Other researches succeed to obtain high PVCR at relatively low operation voltage by suppressing transistor's ON current at the OFF-leakage level with another depletion mode MOSFET or inverter circuit [55]-[56]. In terms of multiple NDR characteristics for MVL and MVM applications, however, it needs more complicated circuit for three-state logic at 3V [57]. In other multiple NDR-based MVL and MVM applications, tri-state latch circuit has been demonstrated by using the series connection of resonant interband tunneling diodes (RITDs) with double-peak based on InAs/AlSb/GaSb at 1.5 V (PVCR = 17) or Si/SiGe with at 3 V (PVCR = 3.25) [58]-[59].

4.2.2 Complementary Double-Peak NDR Characteristics

In this chapter, I propose practical NDR device based on *pn* tunnel junction-embedded conventional Si MOSFET structure having outstanding characteristics of multiple peak and ultra-high PVCR over

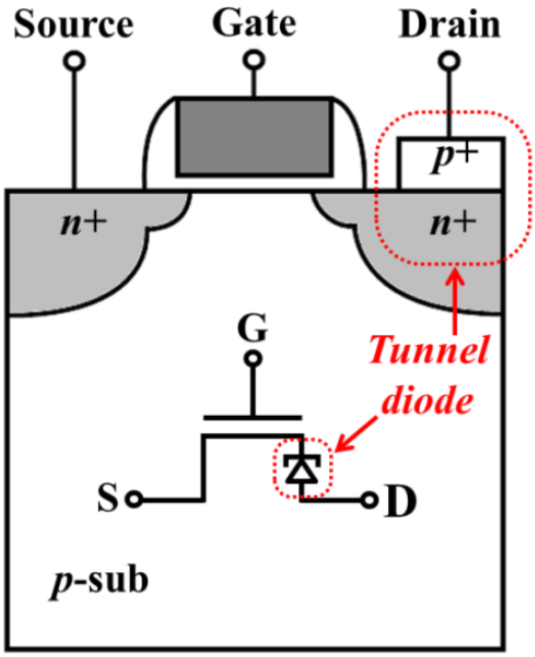


Figure 4.6. Conceptual schematic and symbol of propose NDR device based on tunnel junction-embedded MOSFET

10^6 at 1 V. Figure 4.6 shows the 2D cross-sectional view and circuit symbol of the proposed *n*-type NDR (*n*NDR) device based on the simple *n*-MOSFET structure with a degenerately doped *pn* tunnel junction at the drain side. In our simulation work, complementary *p*-type NDR (*p*NDR) device also can be implemented based on *p*-MOSFET with the tunnel diode [60]-[61].

Figure 4.7(a)-(c) compare the 2D cross-sectional views of conventional HK/MG planar *n*MOS, double-peak *n*NDR device, and T-*n*MOS. The *n*/*p*-type NDR devices have been designed with both *n*+ and *p*+ doping concentration of 1×10^{20} cm^{-3} and a typical junction contact area of 100×100 nm^2 (Fig. 4.7(b)). Compact STI is designed on the conventional binary CMOS inverter with intentionally-high N_{ch} of 2×10^{19} cm^{-3} (Fig. 4.7(c)). Figure 4.7(d)-(f) show the band-to-band generation and recombination rate of each device (Fig. 4.7(a)-(c)). In the NDR device, a normal tunnel (Esaki) diode behavior is observed at on-state MOSFET (V_G=1V), and especially maximum BTBT is generated at the forward bias of 0.35 V (Fig. 4.7(e)). On the other hand, T-CMOS takes advantage of reverse-biased junction BTBT as dominant OFF current mechanism. Only by increasing N_{ch} from 2×10^{18} cm^{-3} to 2×10^{19} cm^{-3}, the maximum BTBT location has been shift from a gate-overlapped LDD region (Fig. 4.7(d)) to a HDD-to-body junction (Fig. 4.7(f)). The conventional CMOS is calibrated by having the experimental ON/OFF current rage of 32 nm HK/MG CMOS characteristics (cf. Fig. 2.6) Device simulation was performed using a Sentaurus^{TM} 3D TCAD device simulator with our numerical BTBT model, default Kane's BTBT model, and field-enhanced TAT model in order to describe forward-biased BTBT, reverse-biased BTBT, and TAT through a forbidden band-gap, respectively [29], [31], [62]-[63]. In

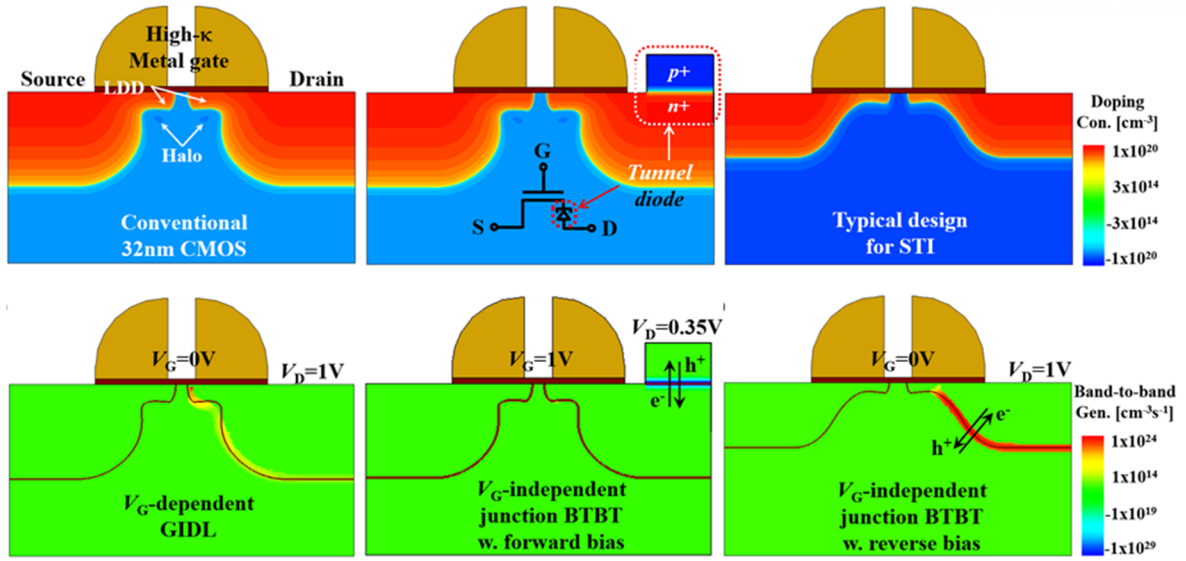


Figure 4.7. Device structure of (a) conventional HK/MG 32nm nMOS, (b) *n*-type NDR (*n*NDR) in tunnel junction-embedded nMOS, and (c) intentionally -high channel doped T-*n*MOS for STI. Band-to-band generation view of (d) conventional *n*MOS, (e) *n*NDR, and (c) T-*n*MOS.

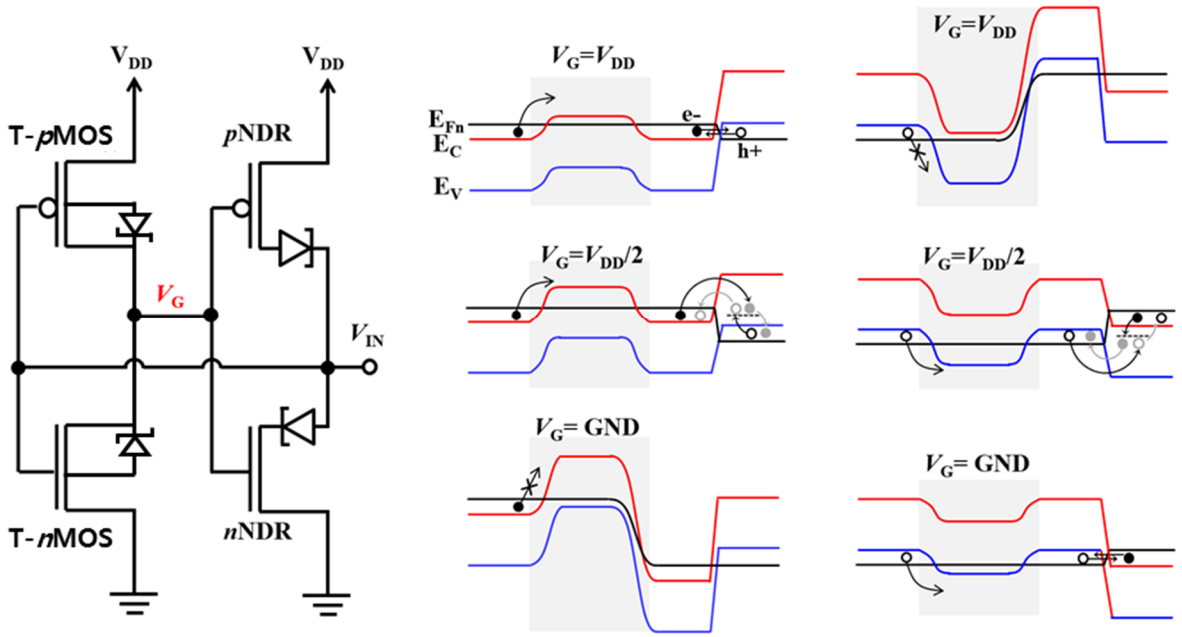


Figure 4.8. (a) Circuit schematics of proposed 5-state latch composed with T-CMOS STI (T-*n*MOS and T-*p*MOS), *n*NDR and *p*-type (*p*NDR). Energy band diagrams of (b) *n*NDR and (c) *p*NDR devices with the carrier (electron/hole) injection mechanism at the "high" ($V_G = V_{DD}$), "intermediate" ($V_G = V_{DD}/2$), and "low" (GND) states of STI.

addition, Fermi-Dirac statistics and band-gap narrowing model also included to calculated degenerately doped Si [64]-[65].

Figure 4.8(a) shows a novel 5-state latch circuit configuration with 4 transistors, *n*/*p*NDR and T-CMOS STI. The compact STI facilitates complement double-peak NDR characteristics with single

input sweep, and accordingly 5-state latch could be implemented in the same unit cell area of binary latch circuit. Figure 4.8(b)-(c) explain the key role of transferred V_G for the complementary operation of multiple *n/p*NDR devices by using energy band diagrams. When the tunnel junction-embedded MOSFET operates at the ON-state (V_G= V_{DD} for *n*NDR and V_G= GND for *p*NDR), it supplies the channel electrons to tunnel diode and then, the first NDR characteristics by the current owing to BTBT, TAT, and diffusion as in a tunnel diode can be obtained. In the OFF-state case (V_G= GND for *n*NDR and V_G= V_{DD} for *p*NDR), high channel potential barrier of MOSFET inhibits the flow of electrons so that the device current can be suppressed at MOSFET OFF-current level. At the "intermediate" (V_G= V_{DD}/2) state, it should be noted that both *n/p*NDR still follow the tunnel diode behaviors with ON-channel *n/p*MOS having threshold voltage ($V_{T,n}$/$V_{T,p}$) below half V_{DD}.

The multiple NDR characteristics can be controlled by design parameters such as doping concentration of tunnel junction and the gate work-function (WF) of the tunnel junction-embedded MOSFET as shown in the Fig. 4.9(a) and (b), respectively. Figure 4.9(a) shows that the currents of first peak (I_{peak1}) and first valley ($I_{valley1}$) by BTBT and TAT increased by field enhancement when the doping concentration of *pn* tunnel junction increased from 1×10^{20} to 5×10^{20} cm^{-3} without changing second NDR characteristics with currents of second peak (I_{peak2}) and second valley ($I_{valley2}$) in this degenerately doping range. These simulated doping-dependent I_{peak1} have been compared to experimental data of Si tunnel junction based on BTBT mechanism [62]. Figure 4.9(b) indicates that the second PVCR can be

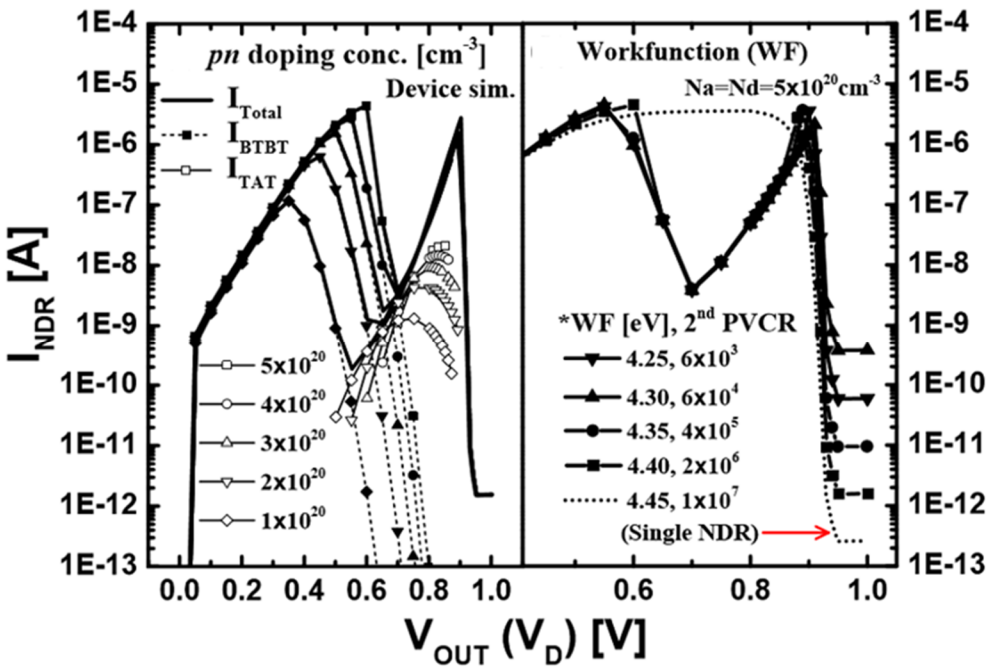


Figure 4.9. Simulation results of *I–V* characteristics with various design parameters: (a) *pn* doping concentrations of tunnel junction and (b) the gate WF of MOSFET in NDR device. The first and second NDR can be controlled by using design parameters of *pn* tunnel junction and MOSFET, respectively.

determined by the OFF-current of the tunnel junction-embedded MOSFET at V_G = 0V, under the condition that the ON-current of the MOSFET is larger than I_{peak1} for first NDR in order to allow the tunneling in the embedded junction. When the V_T of tunnel junction-embedded MOSFET increases by changing the gate WF with 150meV, second PVCR increases from 10^3 to 10^6 since the MOSFET OFF-current ($I_{valley2}$) exponentially decrease by $\exp(-\Delta V_T = mk_BT)$ where m = 1.1~1.4 at T = 300K. Therefore, I can control each first and second NDR by using design parameter of *pn* tunnel junction and its embedded MOSFET, respectively.

4.2.3 Five Memory States of Novel Lath Circuits

Figures 4.10 (a) and (b) show the VTC of T-CMOS STI compared with that of PTI/NTI and consequent multiple-NDR characteristics (I_{NDR}-V_{IN}) with ultra-high PVCR over 10^6 at V_{DD}=1 V based on proposed operation principle where the first peak and valley are generated by a typical tunnel diode

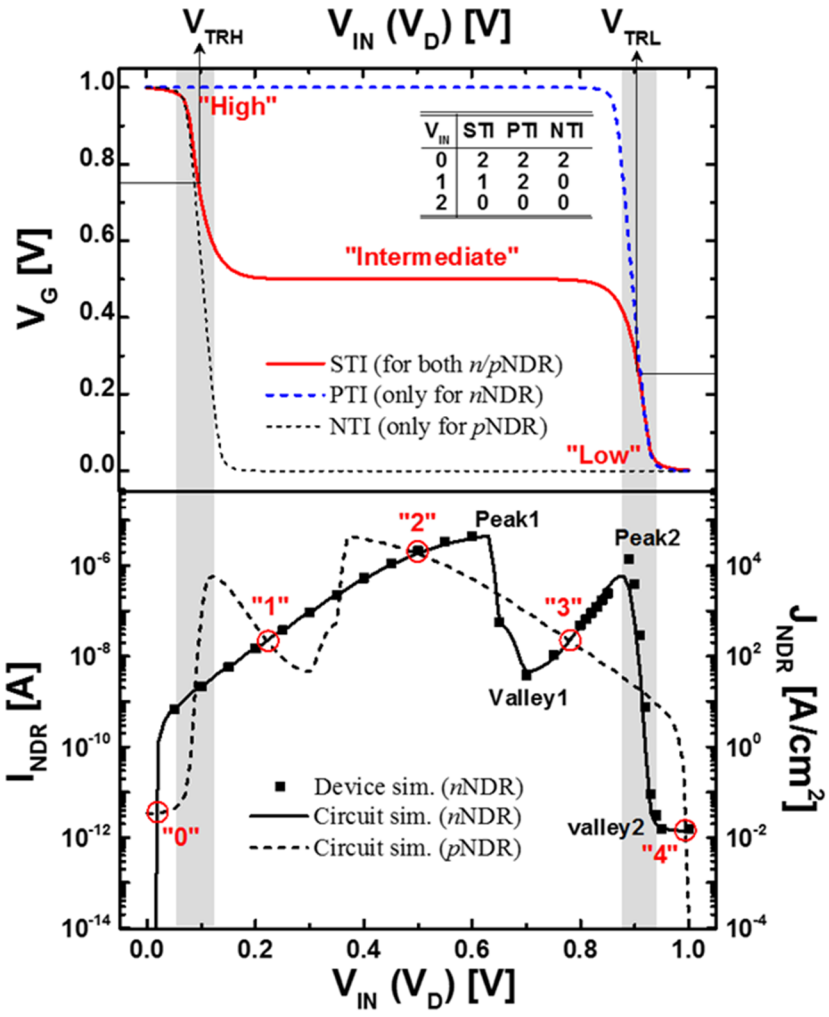


Figure 4.10. Simulation results of (a) VTC of T-CMOS STI comparing with PTI/NTI and (b) corresponding multiple NDR *I-V* characteristics with PVCR over 10^6 at 1V.

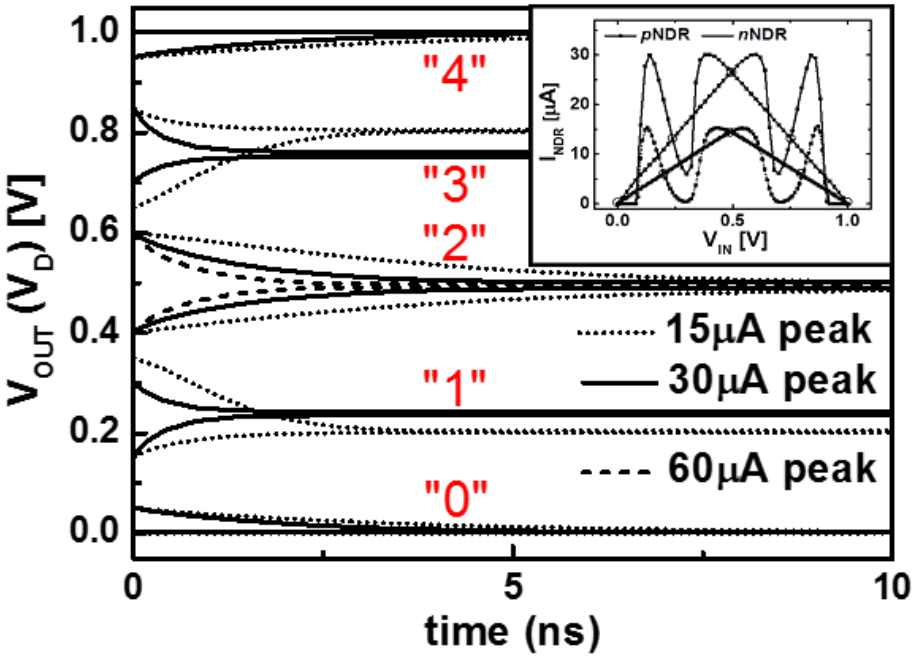


Figure 4.11 Transient simulation results of the latch circuit (Fig. 4.8(a)). Initial states of V_{OUT} with variations of ± 100 mV are converged to 5- states. The dotted line's first peaks and PVCR are referenced by experimental data [50, 68].

behavior and the subsequent second peak can be formed by suppressing the $I_{valley2}$ at the MOSFET OFF-leakage level (~1 pA). The STI can be suppressed $I_{valley2}$ with complementary V_G for each multiple *n*NDR (V_G=0 V) and *p*NDR (V_G=1 V), whereas PTI or NTI can be applied only for multiple *n*NDR or *p*NDR, respectively. The "intermediate"-state (V_G= 0.5 V) of STI plays a key role for compact latch circuit design with 33% area reduction compared with PTI/NTI [(five-state latch with STI and *n/p*NDR) / (five-state latch with PTI, NTI, and *n/p*NDR) = 4 / 6], since it can implement first NDR characteristics in both *n/p*NDR devices by supplying the channel electrons to tunnel diode with V_T of ± 0.1 V. At here, V_{TRH} and V_{TRL} are input voltages where the voltage gain (A_V) become smallest. By obtaining the first peak voltage (V_{peak1}) above V_{DD}/2 with N_D and N_A of 5×10^{20} cm^{-3}, nine crossing points between *n/p*NDR obtained as shown in Fig. 4.10(b). Among of them, five crossing points (red circle) in PDR region become logic or memory states, while other four crossing points in NDR region become boundaries between stable states [66]-[67].

Figure 4.11 shows the transient simulation results of the latch circuit demonstrating five-state latch with only 4 transistors of Fig. 4.8(a). Initial state of V_{IN} with variation of ±100mV are converted to five-state, and its final stable voltages are determined by crossing points. By obtained the V_{peak1} above V_{DD}=2 as in Fig. 4.10, the delay for the "2" state can be comparable with other states since the stable operating point is crossing around the high peak current not the low valley's one. Moreover, the first PVCR

becomes less important than second PVCR in this operating condition. For the realistic delay estimation, Si tunnel diode experimental data have been referenced as the peak current level of 15 μA [68] and first PVCR of 5 [50] in the dotted line results, and the inset of Fig. 4.11 shows the *I-V* characteristics used for transient simulation. As shown in the simulation results with solid and dashed line, delay can be more reduced below 5 ns by increasing the peak currents up to 60 μA. Thus, it can be expected that the speed of five-state MVL/MVM operating can be enhanced further by developing the tunnel junction technology with high peak current density. In terms of power consumption, it should be noted that the MVL/MVM with N states takes the reduced number of bits with $m = \log_N(2^n)$ in comparison with n-bit binary logic for the same amount of data processing ($N^m = 2^n$) [9]. Thus, in case of 5-state MVL/MVM, the 57% reduced number of bit can be obtained from $m = n\log_5(2) = 0.43n$.

Chapter 5. Future Work

5.1 Advanced T-CMOS Technology

The CMOS technology is saturated with giga level (~10^9) due to power scaling limits. To have peta (~10^{14}) level connection (number of synapse in human brain), more power scaling of T-CMOS is required. A peta level connection is expected to have an arithmetic power consumption of 100 kW. Comparing with IBM TrueNorth which consumes 0.1W to synapse connection of 10^8, it requires 1/1000 power saving. Since fabricated T-CMOS is based on very large planar CMOS structure and process with L_G= 1 μm, W= 28 μm, and junction area= 5 μm^2, the measured I_{BTBT} (= area × J_{BTBT}) has 300 pA at V_{DD}= 0.5 V. **Therefore, device scaling based on advanced CMOS technology is essential to reduced I_{BTBT} for ultra-LSTP operation.** In section 3.4, I briefly mentioned strength of bulk ternary FinFET (T-FinFET) structure in terms of SNM based on uniform channel doping. If a low-high channel profile is introduced here, ultra-LSTP T-CMOS with I_{BTBT}= 2 pA can be fabricated as shown in Fig. 5.1

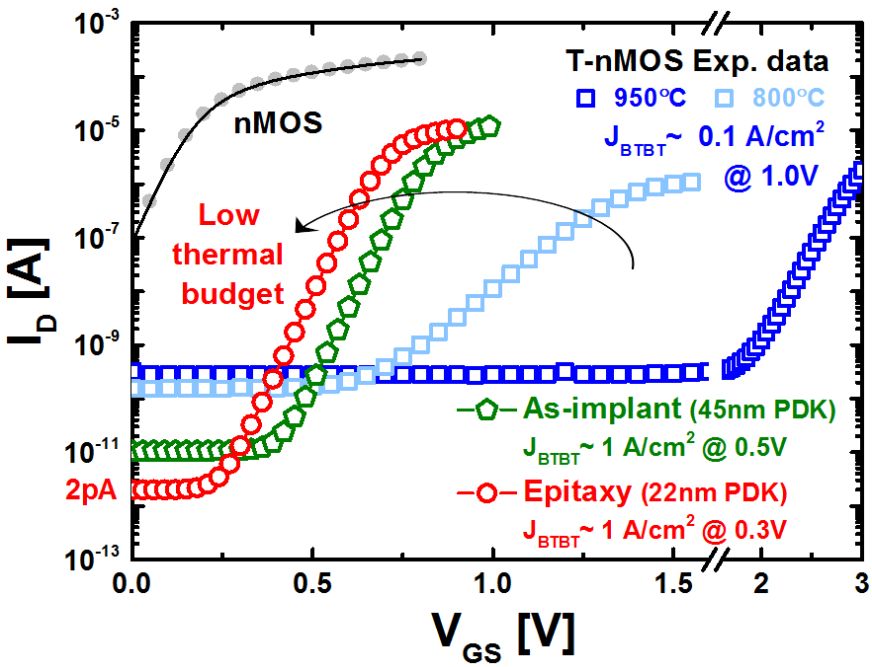


Figure 5.1. Power scaling of T-CMOS applying 45 nm and 22 nm PDK.

5.2 T-CMOS SRAM

In section 4.2, I propose a 5-state latch based on double-peak NDR device and STI circuits. Despite the CMOS-compatible structure, additional processes are inevitable to obtain double-peak NDR characteristics. In the same way as binary 6T-SRAM, ternary SRAM configuration using cross-coupled T-CMOS is practically more feasible. However, there is a restriction on the SNM acquisition problems in the read operation of the T-CMOS SRAM as in the case of binary 6T-SRAM (Fig. 5.2). In the case of CNTFET-based SRAM research [21], the access transistor for read and write is separated to obtain SNM at read operation as shown in Fig. 5.3, which imitates existing binary 8T-SRAM circuits. Therefore, to implement T-CMOS SRAM, it is necessary to study T-CMOS device/circuit to solve SNM problem in read operation is needed.

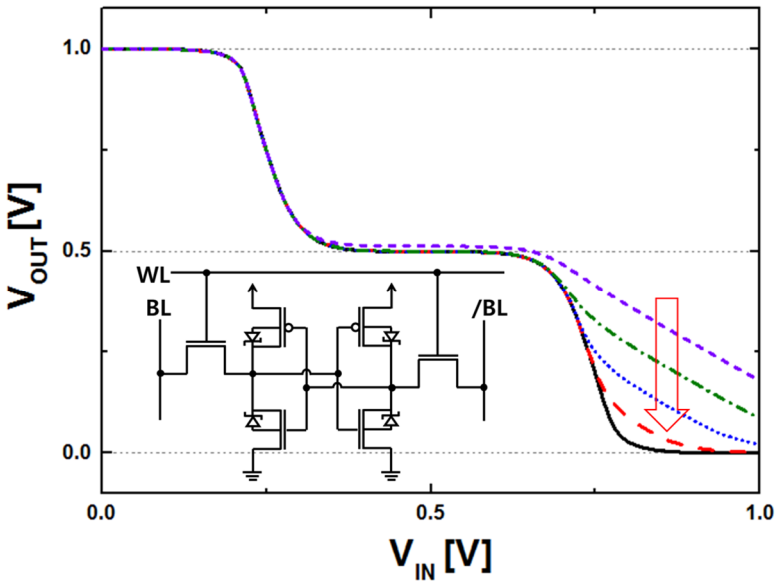


Figure 5.2. Read operation of T-CMOS SRAM. Inset: 6T-TCMOS SRAM circuit configuration.

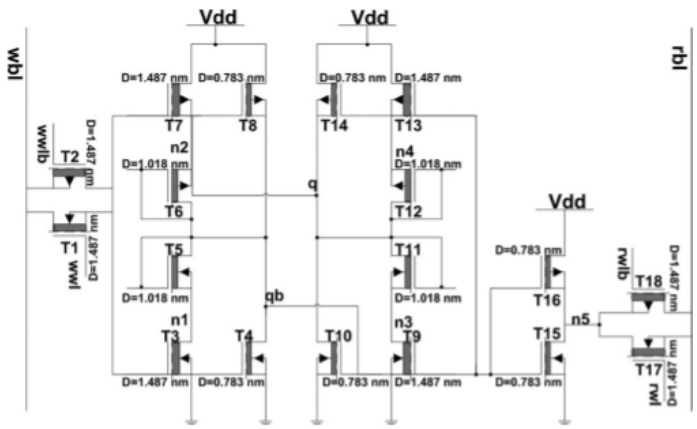


Figure 5.3. CNTFET-based ternary memory cell (transistor level implementation) [21].

5.3 Circuit Design for Ternary Arithmetic Logic Unit.

Using only STI/MIN/MAX gates has limitation to arithmetic logic unit (ALU). In [69], NAOI21, NSHIFT, CARRY, OAI21, and AOI22 gates are proposed to design ternary adder and multiplier as shown in Fig. 5.4. Since the T-CMOS is fully compatible with CMOS technology, it is employed in combination with binary CMOS in the physical-level of design. The ternary logic gates of Fig. 5.4 operate as follows:

$$Y_1(A,B) = \begin{cases} 2 & if\ A = B = 1 \\ (A \wedge B)' & otherwise \end{cases} \tag{5.1}$$

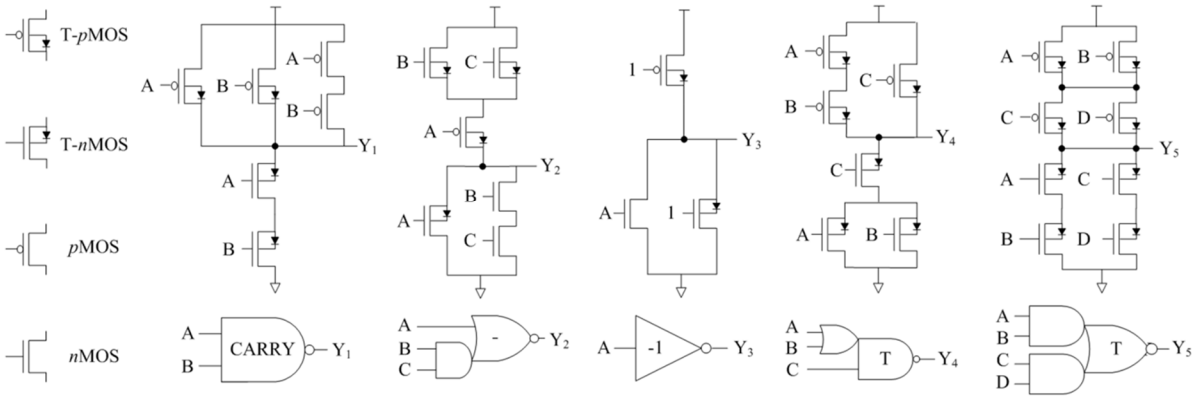
$$Y_2(A,B,C) = \begin{cases} A' & if\ (B \wedge C) = 1 \\ 0 & otherwise \end{cases} \tag{5.2}$$

$$Y_3(A) = \begin{cases} 1 & if\ A = 0 \\ 0 & otherwise \end{cases} \tag{5.3}$$

$$Y_4(A,B,C) = [(A \vee B) \wedge C]' \tag{5.4}$$

$$Y_5(A,B,C,D) = [(A \wedge B) \vee (C \wedge D)]' \tag{5.5}$$

Even though the adder and multiplier can be designed only by using the general MIN/MAX gates, it is necessary to introduce novel ternary logic function with simplified single gate for the better performance and energy efficiency in ternary arithmetic design.



Figrue 5.4. The symbols of (a) T-*n*/*p*MOS and binary *n*/*p*MOS and circuit schematics and its symbols of (b) CARRY, (c) NAOI21, (d) NSHIFT, (d) OAI21, and (e) AOI22 logic gates.

Chapter 6. Conclusion

In this dissertation, I provide feasible and designable ultra-low power T-CMOS device platform for physical synthesis of multi-valued logic and memory applications. Chapter 1 reviewed conventional CMOS problem and present MVL as alternative system. Based on the analysis of MVL research trends and problems, I proposed a novel ternary device concept capable of V_{DD} scaling based on single-V_T and OFF-state constant leading ultra-low P_S and P_D in Chapter 2. By applying a novel ternary device concept to CMOS technology, I confirmed the logic change from binary to ternary based on OFF-state current mechanism of I_{BTBT} and I_{sub} using mixed-mode device simulation. In Chapter 3, the proposed T-CMOS was experimentally demonstrated for the first time and suggested T-CMOS design framework for ultra-low LSTP operation. By developing the compact model of T-CMOS and verifying the physical model parameters with experimental data, compact T-CMOS STI operation has been confirmed and discussed in terms of static noise margin (SNM) and OFF-leakage variation (OLV) from random-dopant fluctuation. In addition, the studies of advanced CMOS technology-based STI to improve SNM and V_{DD} scaling for ultra-low power operation have been conducted. The examples of T-CMOS-based MVL and MVM applications were described in Chapter 4, and future work was present on Chapter 5.

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